MESSAGE FROM THE HON'BLE CHANCELLOR

Dr. P.Shyama Raju
Chancellor
REVA University

REVA University has seen the light of the day to imbibe this character of paradigm shift in academic pursuits to contribute to the knowledge society. REVA works hard to bring in you an exciting and rewarding educational experience, to discover new interests and to develop your career prospects. You will benefit from a unique approach to student-centered learning through group work and individual study tackling real world challenges alongside experienced practitioners and researchers.

REVA has excellent learning facilities including custom built teaching facilities designed specifically to emulate working conditions, air-conditioned library opened for your studies from early morning till midnight and facilities for variety of sports and cultural activities.

Our faculties have introduced socially relevant and market driven engineering courses after studying the requirements of industries in detail and consulting entrepreneurs, experts in different areas of commerce and industry and other stake-holders. I am glad that the Choice Based Credit System (CBCS) and Continuous Assessment Grading Pattern (CAGP) being adopted will facilitate learning environment under continuous guidance and monitoring by the faculty and equip you with competent skills to opt for different job prospects across the global.

I hope that the present scheme of instructions, continuous periodic progress assessments, course curriculum of M.Tech in VLSI and Embedded Systems and other information provided in this hand book will guide you to choose appropriate courses of study and move ahead in the right direction in your chosen area of study. I hope you will enjoy and experience the curriculum, the student-centered teaching and learning ambience in developing your personality to become successful professionals, entrepreneurs and proud citizens of the country.

I wish you every success in your career.

MESSAGE FROM THE HON'BLE VICE-CHANCELLOR

Higher education across the globe is opening doors of its academic disciplines to the real world experiences. The disciplinary legitimacy is under critical review. Trans-border mobility and practice learning are being fore-grounded as guiding principles. Interactive learning, bridging disciplines and facilitating learners to gain different competencies through judicious management of time is viewed as one of the greatest and fascinating priorities and challenges today.

All the programs in REVA University are designed with a great care and after detailed market survey of present requirements and job opportunities. Experts in respective areas of study from primary institutions, industries, research organizations, business sectors and such others have been involved in designing the curriculum of each program.

The L: T: P structure of teaching and learning under Choice Based Credit System (CBCS) and Continuous Assessment Grading Pattern (CAGP) would certainly help our students learn and build competencies needed in this knowledge based society. It provides students an opportunity to choose subject(s) of interest in other areas of study and learn courses with students of different subjects. It facilitates cross cultural learning. It further facilitates students to move in fast track and earn additional certificates and diploma.
The well qualified, experienced, committed teachers in REVA University will involve students in integrative learning and application environment within and outside the university. They will certainly mould them with knowledge, skill and ethical values and empower them to face the competitive world with courage and confidence.

This handy document containing a brief information about M.Tech in VLSI and Embedded Systems, scheme of instruction, course content, CBCS-CAGP regulations and its advantages and calendar of events for the year will serve as a guiding path to students to move forward in a right direction. It is for the students to be disciplined, committed and to work hard and make use of enormous resources and expert faculties to accomplish all round development of their personalities and succeed with flying colours not only in earning degree but also in their future career as leaders and proud citizens of mother India.

Dr. V.G.Talawar
Vice-Chancellor

MESSAGE FROM THE HON'BLE PRINCIPAL DIRECTOR

The curriculum of an institution of higher learning is a living entity. It evolves with time; it reflects the ever changing needs of the society and keeps pace with the growing talent of the students and the faculty. The curriculum of the B. Tech, M.Tech and other programs of REVA University is no exception.

An experience of a decade in preparing graduates and postgraduates in engineering, architecture, law, commerce and science for a wide variety of industries & research level organizations has led to creation of the new curriculum. I sincerely believe that it will meet the aspirations of all stake holders – students, faculty and the employers of the graduates and postgraduates of REVA University.

The curriculum has been designed in such a way that the teacher enjoys freedom to expand it in any direction he feels appropriate and incorporates the latest knowledge and stimulates the creative minds of the students. There is also provision for new experiments with new contents and new techniques. This is going to lead to new teaching – learning paradigm with experiential, experimental & industry relevant approaches. The present curriculum is contemporary because it is culmination of efforts of large number of faculty members, experts from industries and research level organizations. An effort of benchmarking this curriculum with curriculum of other institutions of repute like NITs and IITs has been done.

I am very sure that all students of REVA University enjoy this curriculum and take fullest advantage to expose themselves to fundamentals and applications. Also, imbibe all attributes that are required to term them as Global Engineers. The innovativeness and creativity being introduced should be explored fully by our students.

The flexibility in the curriculum permits staff and students to incorporate changes in terms of addition of new courses and deletion of irrelevant courses keeping the rapid advances in the technology into consideration.

I also record my personal gratitude to Chancellor, Vice chancellor and members of Academic Senate who have lent every bit of their wisdom to make this curriculum truly superior.

Dr. S.Y.Kulkarni
Principal Director - Academics

PREFACE

The M. Tech in VLSI and Embedded System is designed keeping in view the current situation and possible future developments, both at national and international levels. This course is designed to give greater emphasis on VLSI and Embedded System design with a flexibility to explore any of the implementation platform and application field through a number of soft core courses providing knowledge in these specialized areas. This facilitates the students to choose specialized areas of their interest. Adequate attention is given to provide students the basic concepts and requisite skills.

The area of VLSI design has gained enormous popularity over the past few decades due to the rapid advancements in integrated circuit (IC) design and technology. The ability to produce miniaturized circuits with high performance in terms of power and speed is the reason for its popularity. Using ASIC technology, it has been possible to develop high performance multi-core processors. Verification and testing of such complex designs is a critical and challenging task to ensure the quality of the resulting circuits. The advances in EDA software and CAD tools alleviate the effort necessary to carry out the cumbersome design and verification process of ICs.

The program is designed to expose students to various courses having applications in VLSI and Embedded System like Digital VLSI design, ASIC design, SOC design, Low Power VLSI, High Speed VLSI design, VLSI Testing and verification, CMOS RF Circuit design, Low Power Embedded system. They are also exposed to basic concepts of NANO technology, VLSI testing and Verification, fabrication process ,MEMS, Application specific design and embedded platform like ARM, MSP430, low power microcontrollers and FPGA, through outcome based teaching and learning process which emphasizes practical exposure rather than memorization. A variety of activities such as mini projects, seminars, internships, certification programs, etc. in consultation with industries will be carried out. There is also a scope for cultural, social and community service activities for the students to shape their personality suitable for all-round development.

The VLSI and Embedded System students can choose their career in any VLSI and Embedded System development industries. Now a days almost every appliance is coming with some VLSI component. The scope of VLSI and Embedded System is very wide covering almost every home appliances, industry, automotives, and medical appliance manufactures industry automation and control, telecommunication, Computer and Digital Systems, defense and space exploration.

I am sure the students choosing M Tech in VLSI and Embedded System in School of Electronics and Communication Engineering in REVA University will enjoy the curriculum, teaching and learning environment, the vast infrastructure and the experienced teachers involvement and guidance. We will strive to provide all needed comfort and congenial environment for their studies. I wish all students pleasant stay in REVA and grand success in their career.

Prof. Rajashekhar C. Biradar
Director
School of Electronics and Communication Engineering

CONTENTS

RUKMINI EDUCATIONAL CHARITABLE TRUST

It was the dream of late Smt. Rukmini Shyama Raju to impart education to millions of underprivileged children as she knew the importance of education in the contemporary society. The dream of Smt. Rukmini Shyama Raju came true with the establishment of Rukmini Educational Charitable Trust (RECT), in the year 2002. **Rukmini Educational Charitable Trust** (RECT) is a Public Charitable Trust, set up in 2002 with the objective of promoting, establishing and conducting academic activities in the fields of Arts, Commerce, Education, Engineering, Environmental Science, Management and Science & Technology, among others. In furtherance of these objectives, the Trust has set up the REVA Group of Educational Institutions comprising of REVA Institute of Technology & Management (RITM), REVA Institute of Science and Management (RISM), REVA Institute of Management Studies (RIMS), REVA Institute of Education (RIE), REVA First Grade College (RFGC), REVA Degree College (Evening), REVA Independent PU College at Kattigenahalli, Ganganagar and Sanjaynagar and now REVA University. Through these institutions, the Trust seeks to fulfill its vision of providing world class education and create abundant opportunities for the youth of this nation to excel in the areas of Engineering, Commerce, Management, Education, Arts and Science & Technology.

Every great human enterprise is powered by the vision of one or more extraordinary individuals and is sustained by the people who derive their motivation from the founders. The Chairman of the Trust is Dr. P. Shyama Raju, a developer and builder of repute, a captain of the industry in his own right and the Chairman and Managing Director of the DivyaSree Group of companies. The idea of creating these top notch educational institutions was born of the philanthropic instincts of Dr. P. Shyama Raju to do public good, quite in keeping with his support to other socially relevant charities such as maintaining the Richmond road park, building and donating a police station, gifting assets to organizations providing accident and trauma care, to name a few.

The Rukmini Educational Charitable Trust drives with the main aim to help students who are in pursuit of quality education for life. REVA is today a family of ten institutions providing education from PU to Post Graduation and Research leading to M. Phil and PhD degrees. REVA has well qualified experienced teaching faculty of whom majority are doctorates. The faculty is supported by committed administrative and technical staff. Over 9,000 students study various courses across REVA's three campuses equipped with exemplary state-of-the-art infrastructure and conductive environment for the knowledge driven community.

ABOUT REVA UNIVERSITY

REVA University established under the Government of Karnataka Act 80 of the year 2012 and notified in the Karnataka Gazette dated 7th Feb, 2013, is located 22 kms away from the Bangalore International Airport on the way to Bangalore city. The university has a sprawling lush green campus spread over 42 acres of land equipped with state-of-the-art infrastructure and conductive environment for higher learning.

The REVA campus has well equipped laboratories, custom-built teaching facilities designed specifically to emulate working conditions, fully air-conditioned library and central computer center kept open from morning 8.00 AM till mid-night for the students and the faculty. The well planned sports facility for variety of sports activities, facilities for cultural programs and friendly campus lifestyle add to the overall personality development of students. The campus also has residential facility for students, faculty and other staff.

Currently, REVA University offers 18 Post Graduate programs and 8 Graduate programs in Engineering and Technology, Science, Commerce and Management in addition to research degrees leading to PhD in different disciplines. The University aims to offer many more PG and UG programs in Science, Arts, Commerce, Engineering & Technology, Management Studies, Education, in the years to come.

The programs being offered by the REVA University are well planned and designed after detailed study with emphasis with knowledge assimilation, applications, global job market and their social relevance. Highly qualified, experienced faculty and scholars from reputed universities / institutions, experts from industries and business sectors have contributed in preparing the scheme of instruction and detailed curricula for this program. Greater emphasis on practice in respective areas and skill development to suit to respective job environment has been given while designing the curricula. The Choice Based Credit System and Continuous Assessment Graded Pattern (CBCS – CAGP) of education has been introduced in all programs to facilitate students to opt for subjects of their choice in addition to the core subjects of the study and prepare them with needed skills. The system also allows students to move forward under the fast track for those who have the capabilities to surpass others. These programs are taught by well experienced qualified faculty supported by the experts from industries, business sectors and such other organizations. REVA University has also initiated many supportive measures such as bridge courses, special coaching, remedial classes, etc., for slow learners so as to give them the needed input and build in them confidence and courage to move forward and accomplish success in their career. The University has also entered into MOUs with many industries, business firms and other institutions seeking their help in imparting quality education through practice, internship and also assisting students' placements.

ABOUT SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

The School of Electronics and Communication Engineering headed by a highly experienced Professor and is supported by well qualified faculty members. The school has the state-of-art class rooms and well equipped laboratories. It offers B.Tech and M.Tech programs in various specialized streams. The school also has research program leading to doctoral degree. The curriculum of both graduate and post graduate degree programs have been designed to bridge the gap between industry – academia and hence they are industry application oriented. The B. Tech program aims to prepare human resources to play a leading role in the continuing adventure of modern automated systems and communications. The Master degree programs focus on research and design in the core and IT industries, building and marketing the next generation of product development. This is reflected in various core subjects offered within the program. B. Tech program offers numerous choices of study for the students based on interest in the current state of art technology. Apart from fundamental courses in Electronics and Communication Engineering, the school facilitates to study in four streams such as Circuits and Devices, Communication Engineering, Signal Processing and Programming. Students are at liberty to choose from these streams in higher semesters. However, there is no restriction of cross migration from one stream to another at any level and thus there is a flexibility provided in the course duration.

The faculty members have number of publications in reputed national and international journals/conferences. The school is also involved in funded research projects. The other important features of the school are individual counseling of students for academic performance, additional coaching classes for important subjects for all the semesters, soft skill development classes, scientific and student centered teaching-learning process.

Student's welfare is given utmost priority here at School of Electronics and Communication Engineering. Advanced learning methods are adopted to make learning truly interactive. More focus is on discussion and practical applications rather than rote learning. Notes/handouts are given and critical thinking questions are asked to test understanding. Experienced, well qualified and friendly faculty members always strive hard to provide best of education to students.

Vision

The School of Electronics and Communication Engineering is envisioned to be a leading centre of higher learning with academic excellence in the field of electronics and communication engineering blended by research and innovation in tune with changing technological and cultural challenges.

Mission

- Establish a unique learning environment to enable the students to face the challenges of the Electronics and Communication Engineering field.

- Promote the establishment of centers of excellence in niche technology areas to nurture the spirit of innovation and creativity among faculty and students.
- Provide ethical and value based education by promoting activities addressing the societal needs.
- Enable students to develop skills to solve complex technological problems of current times and also provide a framework for promoting collaborative and multidisciplinary activities.

Program Educational Objectives (PEO's)

The programme educational objectives of the Electronics and Communication Engineering of REVA University is to prepare graduates

PEO-1	To have successful professional careers in national and multinational organization and communicate effectively as a member of a team or to lead a team.
PEO-2	To continue to learn and advance their careers through activities such as research and development, acquiring doctoral degree, participation in national level research programmes, teaching and research at university level etc.,
PEO-3	To be active members ready to serve the society locally and internationally, may take up entrepreneurship for the growth of economy and to generate employment; and adopt the philosophy of lifelong learning to be aligned with economic and technological development.

Program Outcomes (POs)

After successful completion of the programme, the graduates shall be able to

PO1. **Demonstrate in-depth knowledge** of VLSI and Embeded Systems, including wider and global perspective, with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge, and integration of the same for enhancement of knowledge.

PO2. **Analyze complex engineering problems critically**, apply independent judgment for synthesizing information to make intellectual and/or creative advances for conducting research in a wider theoretical, practical and policy context.

PO3. **Think laterally and originally, conceptualize and solve engineering problems, evaluate** a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.

PO4. **Extract information pertinent to unfamiliar problems through literature survey and experiments**, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze and interpret data, demonstrate higher order skill and view things in a broader perspective, contribute individually/in group(s) to the development of scientific/technological knowledge in one or more domains of engineering.

PO5. **Create, select, learn and apply appropriate techniques**, resources, and modern engineering and IT tools, including prediction and modeling, to complex engineering activities with an understanding of the limitations.

PO6. **Possess knowledge and understanding of group dynamics, recognize** opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.

PO7**. Demonstrate knowledge and understanding** of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economical and financial factors.

PO8. **Communicate with the engineering community, and with society at large**, regarding **complex engineering activities** confidently and effectively, such as, being able to comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

PO9: **Recognize the need for**, and have the preparation and ability to engage in **life-long learning** independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

PO10. **Acquire professional and intellectual integrity,** professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PO11. **Observe and examine critically the outcomes** of one's actions and make corrective measures subsequently, and learn from mistakes without depending on external feedback (**SELF learning**)

Programme Specific Outcomes (PSO's)

After successful completion of the programme, the graduates shall be able to

1. Isolate and solve complex problems in the domains of VLSI and Embedded Systems using latest hardware and software tools and technologies, along with analytical and managerial skills to arrive at cost effective and optimum solutions either independently or as a team.
2. Implant the capacity to apply the concepts of FPGA, ASIC, System On Chip, IoT and cyber physical systems, etc. in the design, development and implementation of application oriented engineering systems
3. Design, Model, Analyze and VLSI and Embedded Systems to solve real life and industry problems.

Board of Studies for School of Electronics and Communication Engineering

Sl. No.	Name, Designation & Affiliation	Status
1	**Dr. R. C. Biradar** Director, School of ECE, Reva University, Bangalore	**Chair Person**
2	**Dr. Rathna G. N.** Principal Research Scientist, E&E Dept., IISc., Bangalore	**Member**
3	**Dr.Vasantha M. H.** HOD, Dept. of ECE, NIT,Goa	**Member**
4	**Dr. VaibhavMeshram** Director,Jain University, Bangalore	**Member**
5	**Mr. Chandra Mohan** CEO, Goshakthi Renewable, Bangalore	**Member**
6	**Dr. K. S. Gurumurthy** Senior Professor, School of ECE, Reva University	**Member (Internal)**
7	**Dr. Venkata Siva Reddy** Professor, School of ECE, Reva University	**Member (Internal)**
8	**Dr. Bharathi S. H.** Professor, School of ECE, Reva University	**Member (Internal)**
9	**Prof.Jayaraman K.** Adjunct Professor, School of ECE,Reva University	**Member (Internal)**
10	**Dr. Geetha D. D.** Professor, School of ECE, Reva University	**Member (Internal)**
11	**Dr. P. I. Basarkod** Professor, School of ECE, Reva University	**Member (Internal)**

Advisory Board for School of Electronics and Communication Engineering

Sl.No	Name and affiliation
1	Dr. M.H.Kori, Technology Consultant, Technology Adviser Validus Technologies USA, Retd. Technical Director, Alcatel-Lucent Technologies, Bangalore
2	Dr. Vinod Sharma Professor, ECE Department, IISc. Bangalore
3	Dr. Surendra Pal Former ISRO Scientist, President, IETE-India, Bangalore
4	Dr. Shirshu Varma Professor, Department of Computer Science and Engineering IIIT Allahabad
5	Dr. Rathna Principal Research Scientist, Department of Electrical Engineering IISc., Bangalore
6	Dr. ArzadAlamKherani Samsung R and D, Bangalore
7	Dr. MahadevPrasanna Department of Electrical and Electronics Engineering IIT Guwahathi
8	Dr. Muralidhara Kulkarni Department of Electronics & Communication Engineering, NITK, Surathkal
9	Dr. Kumarashama Department of Electronics & Communication Engineering, Manipal Institute of Technology, Manipal
10	Dr.Vijayaprakash Department of Electronics & Communication Engineering, Bangalore Institute of Technology, Bangalore
11	Mr.Aravinda Sharma, Manager,Delphi Systems, Bangalore
12	Dr. Kashinath, Director, ALS Semiconductors, Bangalore
13	Mr.LokeshaRai K, Director, Symphony Telecca Services, Bangalore
14	Mrs.Deepa, Senior Engineer, Intel Corporation,Bangalore

CBCS (CHOICE BASED CREDIT SYSTEM) AND CAGP (CONTINUOUS ASSESSMENT AND GRADING PATTERN) OF EDUCATION AND ITS ADVANTAGES

CBCS is a proven, advanced mode of learning in higher education. It facilitates students to have freedom in making their own choices for acquiring a Degree / Masters Degree program. It is more focused towards the student's choice in providing a wide range of modules available in a single campus across various disciplines offered by experts in the subjects. It leads to quality education with active teacher-student participation.

Studying under CBCS has following advantages:

- Students may undergo training in cross-disciplinary and multi-disciplinary subjects and acquire more focused and preferred knowledge.
- Students may get more skills from other subject(s) which are required for the career path in addition to their regular subject knowledge.
- Students may get ample opportunities to use the laboratories and gain practical exposure to the much needed modules available in other departments/schools for want of scientific inputs.
- Courses are conducted by subject experts identified on the basis of their experiences. Courses taught by such experts may provide in-depth information and clear understanding of the modules.
- Students may get an opportunity to study courses with other students of different programs and exchange their views and knowledge in a common class room.
- CBCS provides a cross-cultural learning environment.
- Students may benefit much from selecting the right options to successfully face the public service examinations like UPSC, KPSC, IFS, IES wherein the knowledge of additional subjects become mandatory for general or optional papers.
- Students are exposed to the culture of universal brotherhood during their campus life.
- Students are allowed to practice various methods of learning a subject.

Brief Summary of REVA University Regulations for Choice Based Credit System (CBCS) and Continuous Assessment Grading Pattern (CAGP) for Engineering Degree Program

1.0 Teaching and Learning Process

The teaching and learning process under CBCS-CAGP of education in each course of study will have three components, namely,

(i) L= Lecture (ii) T= Tutorial (iii) P= Practice, where:

L stands for **Lecture** session consisting of classroom instruction.

T stands for **Tutorial** session consisting participatory discussion / self-study/ desk work/ brief seminar presentations by students and such other novel methods that make a student to absorb and assimilate more effectively the contents delivered in the Lecture classes.

P stands for **Practice** session and it consists of Hands on Experience / Laboratory Experiments / Field Studies / Case Studies that equip students to acquire the much required skill component.

2.0 Course of Study and Duration:

The study of B Tech degree is grouped under various courses. Each of these course carries credits which are based on the number of hours of teaching and learning. In the teaching-learning process every **one hour session of L amounts to 1 credit per Semester.** In case of **T or P** minimum of **two hour session amounts to 1 credit or a three hour session amounts to 2 credits per semester of 16 weeks.**

The total duration of a semester is 20 weeks inclusive of semester-end examination.

A course shall have either or all the three components. That means a course may have only lecture component, or only practical component or combination of any two or all the three components.

2.1. Various course of s**tudy** are labeled and defined as: (i) Core Course (CC), (ii) Hard Core Course (HC), (iii) Soft Core Course (SC), (iv) Foundation Core Course (FC) and (v) Open Elective Course (OE).

(i) **Core Course:** A course which should compulsorily be studied by a candidate as a core-requirement is termed as a Core course.

(ii) Foundation Course (FC):
The foundation Course is a core course which should be completed successfully as a part of graduate degree program irrespective of the branch of study.

(iii) Hard Core Course (HC):
The **Hard Core Course** is a Core Course in the main branch of study and related branch(es) of study, if any that the candidates have to complete compulsorily.

(iv) Soft Core Course (SC):
A Core course may be a **Soft Core** if there is a choice or an option for the candidate to choose a course from a pool of courses from the main branch of study or from a sister/related branch of study which supports the main branch of study.

(v) O**pen Elective Course:**
An elective course chosen generally from other discipline / subject, with an intention to seek exposure is called an O**pen Elective Course.**

2.2. Project Work:

Project work is a special course involving application of knowledge in solving / analyzing /exploring a real life situation / difficult problem.

2.3. Minor Project:

A project work up to **FOUR to SIX** credits is called **Minor Project** work. A Minor Project work may be a hard core or a Soft Core as decided by the BoS / concerned.

2.4. Major Project / Dissertation:

A project work of **EIGHT, TEN, TWELVE or SIXTEEN** credits is called **Major Project** work. The Major Project / Dissertation shall be Hard Core.

3.0. Minimum Credits to be Earned:

3.1. A candidate has to earn 192 credits for successful completion of B Tech degree with a distribution of credits for different courses as prescribed by the university.

3.2. A candidate can enroll for a maximum of 32 credits per Semester. However he / she may not successfully earn a maximum of 32 credits per semester. This maximum of 32 credits does not include the credits of courses carried forward by a candidate.

3.3. Only such full time candidates who register for a minimum prescribed number of credits in each semester from I semester to VIII semester and complete successfully 192 credits in 8 successive semesters shall be considered for declaration of Ranks, Medals, Prizes and are eligible to apply for Student Fellowship, Scholarship, Free ships, and such other rewards / advantages which could be applicable for all full time students and for hostel facilities.

4.0. Add- on Proficiency Certification:
In excess to the minimum of 192 credits for the B. Tech Degree program, a candidate can opt to complete a minimum of 4 extra credits either in the same discipline/subject or in different discipline / subject to acquire **Add on Proficiency Certification** in that particular discipline / subject along with the B. Tech. degree.

4.1. Add on Proficiency Diploma:
In excess to the minimum of 192 credits for the B. Tech degree program, a candidate can opt to complete a minimum of 18 extra credits either in the same discipline/subject or in different discipline / subject to acquire Add on Proficiency Diploma in that particular discipline / subject along with the B. Tech degree. The **add-on proficiency certification / diploma** so issued to the candidate contains the courses studied and grades earned.

5.0. Continuous Assessment, Earning of Credits and Award of Grades.

5.1. The assessment and evaluation process happen in a continuous mode. However, for reporting purpose, **a semester is divided into 3 components as C1, C2, and C3.**

The performance of a candidate in a course will be assessed for a maximum of 100 marks as explained below.

(i) Component C1:

The first Component (C1), of assessment is for 25 marks. This will be based on test, assignment / seminar. During the first half of the semester (i.e. by 8th week), the first 50% of the syllabus (Unit 1&2) will be completed. This shall be consolidated during the first three days of 8th week of the semester. A review test based on C1 will be conducted and completed in the beginning of the 9th week. In case of courses where test cannot be conducted, the form of assessment will be decided by the concerned school and such formalities of assessment will be completed in the beginning of the 9th week. The academic sessions will continue for C2 immediately after completion of

process of C1.

The finer split - up for the award of marks in C1 is as follows:
Assignment / Seminar..... 5 marks for Unit 1&2
Test (Mid-Term).....20 marks for Unit 1&2
Total ..... 25 marks

(ii) Component C2:

The second component (C2), of assessment is for 25 marks. This will be based on test, assignment /seminar. The continuous assessment and scores of second half of the semester (9th to 16th week) will be consolidated during 16th week of the semester. During the second half of the semester the remaining units in the course will be completed. A review test based on C2 will be conducted and completed during 16th week of the semester. In case of courses where test cannot be conducted, the form of assessment will be decided by the concerned school and such formalities of assessment will be completed during 16th week.

The 17th week will be for revision of syllabus and preparation for the semester - end examination.
The finer split - up for the award of marks in C2 is as follows:
Assignment / Seminar..... 5 marks for Unit 3 & 4
Review Test (Mid-Term)..... 20 marks for Unit 3 & 4
Total .....25 marks

(iii) Component C3:

The end semester examination of 3 hours duration for each course shall be conducted during the 18th & 19th week. **This forms the third / final component of assessment (C3) and the maximum marks for the final component will be 50.**

5.2. Evaluation of Minor Project / Major Project / Dissertation:

Right from the initial stage of defining the problem, the candidate has to submit the progress reports periodically and also present his/her progress in the form of seminars in addition to the regular discussion with the supervisor. At the end of the semester, the candidate has to submit final report of the project / dissertation, as the case may be, for final evaluation. The components of evaluation are as follows:

Component – I	(C1)	Periodic Progress and Progress Reports (25%)
Component – II	(C2)	Results of Work and Draft Report (25%)
Component– III	(C3)	Final Evaluation and Viva-Voce (50%). Evaluation of the report is for 30% and the Viva-Voce examination is for

5.3. The details of continuous assessment are summarized in the following table:

Component	Period	Syllabus	Weightage	Activity
C1	1st Week to 8th Week			Instructional process and Continuous Assessment
	Last 3 days of 8thWeek	First 50% (two units)	25%	Consolidation of C1
C2	From first day of 9th Week to first 3 days of16th Week			Instructional process and Continuous Assessment
	Last 3 days of 16th Week	Second 50% remaining two units	25%	Consolidation of C2
C3	17th Week			Revision and preparation for Semester–end exam(C3)
	18th Week to 19th Week	Entire syllabus	50%	Conduct of Semester-end Exams (C3)
	20th Week			Evaluation and Tabulation
	End of 20th Week			Notification of Final Grades

Note: Practical examination wherever applicable shall be conducted before conduct of C2 Examination. The calendar of practical examination shall be decided by the respective school.

A candidate's performance from all 3 components will be in terms of scores, and the sum of all three scores will be for a maximum of 100 marks (25 + 25 + 50).

5.4. Provision for Make- up Examination:

For those students who have secured less than 40% marks in end semester examination (C3) the university shall conduct a make-up examination after the end of every semester and before the commencement of next subsequent semester.

Such of those students who have secured more than 30% marks in C1 and C2 together and less than 40% marks in the End Semester Examination (C3) in a given course shall appear for make-up examination in that course.

A student who is absent to End Semester Examination (C3) due to medical emergencies or such other exigencies and fulfills the minimum attendance and performance requirements in C1 & C2 shall appear for make-up examination.

6.0. Re-Registration and Re-Admission:

In case a candidate fails in more than 4 courses in odd and even semesters together in a given academic year has to seek re-admission to those semesters during subsequent year within a stipulated period.

In case a candidate's class attendance in aggregate of all courses in a semester is less than 75% or as stipulated by the University, such a candidate is not allowed to appear for end semester examination (C3) and he / she shall have to seek re-admission to that semester during subsequent year within a stipulated period.

6.1. In such case a candidate drops all the courses in semester due to personal reasons he / she can take re-admission to such dropped semester.

6.2 Provision to carry forward the failed subjects / courses:

The student who has failed in 4 courses in odd and even semesters together shall move to next semester of immediate succeeding year of study. And he / she shall appear for C3 examination of failed courses of previous semesters concurrently with odd and even end semester examinations (C3) of current year of study. However, he / she shall have to clear all courses of both odd and even semesters of preceding year to register for next succeeding semester.

Examples:-

1) Student "A" has failed in one course in first semester and 3 courses in second semester. He / she is eligible to seek admission for third semester and appear for C3 examination of one failed course of first semester concurrently with third semester C3 examination. Likewise, he / she is eligible to appear for C3 examination of 3 failed courses of second semester concurrently with fourth semester C3 examination. However, he / she has to clear all the failed courses of first and second semesters before seeking admission to fifth semester.

2) Student "B" has failed in two courses in third semester and two courses in fourth semester and has passed in all courses of first and second semesters. He / she is eligible to seek admission to fifth semester and appear for C3 examination of two failed courses of third semester concurrently with fifth semester C3 examination. Likewise he / she is eligible to appear for C3 examination of two failed courses of fourth semester concurrently with sixth semester C3 examination. However, he / she is not eligible to seek admission to seventh semester unless he / she passes in all the failed courses of third and fourth semesters.
3) Student "C" has failed in four courses in first semester but has cleared all the courses in second semester. He / she is eligible to seek admission for third semester and appear for C3 examination of four failed courses of first semester concurrently with third semester C3

examination. However, he / she is not eligible to seek admission for fifth semester unless he / she clears all the four failed courses of first semester.

7.0. Attendance Requirement:

a) All students must attend every lecture, tutorial and practical classes.
b) In case a student is on approved leave of absence (e g:- representing the university in sports, games or athletics, placement activities, NCC, NSS activities and such others) and / or any other such contingencies like medical emergencies, the attendance requirement shall be minimum of 75% of the classes attended.
c) Any student with less than 75% of attendance in a course in aggregate during a semester shall not be permitted to appear to the end semester (C3) examination.
d) Teachers offering the courses will place the above details in the School / Department meeting during the last week of the semester, before the commencement of C3, and subsequently a notification pertaining to the above will be brought out by the Head of the School before the commencement of C3 examination. A copy of this notification shall also be sent to the office of the Registrar & Registrar (Evaluation).

7.1. Absence during mid-semester examination:

In case a student has been absent from a mid-semester examination due to the illness or other contingencies he / she may give a request along with necessary supporting documents and certification from the concerned class teacher / authorized personnel to the concerned Head of the School, for make-up examination. The Head of the School may consider such request depending on the merit of the case and after consultation with course instructor and class teacher, and permit such student to appear for make-up mid semester examination.

7.2. Absence during end semester examination:

In case a student is absent for end semester examination on medical grounds or such other exigencies, the student can submit request for make-up examination, with necessary supporting documents and certification from the concerned class teacher / authorized personnel to the concerned Director of the School. The Director of the School may consider such request depending on the merit of the case and after consultation with class teacher, course instructor and permit such student to appear for make-up mid semester examination

8.0. Challenge Valuation

A student who desires to apply for challenge valuation shall obtain a photo copy of the answer script by paying the prescribed fee within 10 days after the announcement of the results. He / She can challenge the grade awarded to him/her by surrendering the grade card and by submitting an application along with the prescribed fee to the Registrar (Evaluation) within 07days after the announcement of the results. This challenge valuation is only for C3 component.

The answer scripts for which challenge valuation is sought for shall be evaluated by

the external examiner who has not involved in the first evaluation. The higher of two marks from first valuation and challenge valuation shall be the final.

9.0. Provisional Grade Card: The tentative / provisional grade card shall be issued by the Registrar (Evaluation) at the end of every semester indicating the courses completed successfully. The provisional grade card provides **Semester Grade Point Average** (SGPA). The SGPA is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.

SGPA (Si) = ∑ (Ci x Gi) / ∑Ci

Where Ci is the number of credits of the i^{th} course and Gi is the grade point scored by the student in the i^{th} course.

9.1. Final Grade Card: Upon successful completion of B Tech Degree a Final Grade card consisting of Grades of all courses successfully completed by the candidate will be issued by the Registrar (Evaluation).

9.2. The Grade and the Grade Point: The Grade and the Grade Point earned by the candidate in the subject will be as given below.

Marks P	Grade G	Grade Point (GP=V x G)	Letter Grade
90-100	10	v*10	O
80-89	9	v*9	A
70-79	8	v*8	B
60-69	7	v*7	C
50-59	6	v*6	D
40-49	5	v*5	E
0-39	0	v*0	F

O - Outstanding; A-Excellent; B-Very Good; C-Good; D-Fair; E-Satisfactory; F - Fail;

Here, P is the percentage of marks (P= [(C1+C2) +M] secured by a candidate in a course which is **rounded to nearest integer**. V is the credit value of course. G is the grade and GP is the grade point.

9.3. Cumulative Grade Point Average (CGPA):

Overall Cumulative Grade Point Average (CGPA) of a candidate after successful completion of the required number of credits (192) for B. Tech degree in Engineering & Technology is calculated taking into account all the courses undergone by a student over

all the semesters of a program, i.e. : **CGPA = ∑ (Ci x Si) / ∑Ci**
Where Si is the SGPA of the i^{th} semester and Ci is the total number of credits in that semester.

The SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

CONVERSION OF GRADES INTO PERCENTAGE:
Conversion formula for the conversion of CGPA into Percentage is:
Percentage of marks scored = CGPA Earned x 10
Illustration: CGPA Earned 8.10 x 10 = 81.0

10.0 Classification of Results

The final grade point (FGP) to be awarded to the student is based on CGPA secured by the candidate and is given as follows.

CGPA	FGP	
	Numerical Index	Qualitative Index
> 4 CGPA < 5	**5**	SECOND CLASS
5 > = CGPA < 6	6	
6 >= CGPA < 7	7	FIRST CLASS
7 >= CGPA < 8	8	
8 >= CGPA < 9	9	DISTINCTION
9 >= CGPA 10	10	

Overall percentage=10*CGPA

11.0. Provision for Appeal

If a candidate is not satisfied with the evaluation of C1 and C2 components, he/she can approach the grievance cell with the written submission together with all facts, the assignments, and test papers etc., which were evaluated. He/she can do so before the commencement of semester-end examination. The grievance cell is empowered to revise the marks if the case is genuine and is also empowered to levy penalty as prescribed by the university on the candidate if his/her submission is found to be baseless and unduly motivated. This cell may recommend taking disciplinary/corrective action on an evaluator if he/she is found guilty. The decision taken by the grievance cell is final.

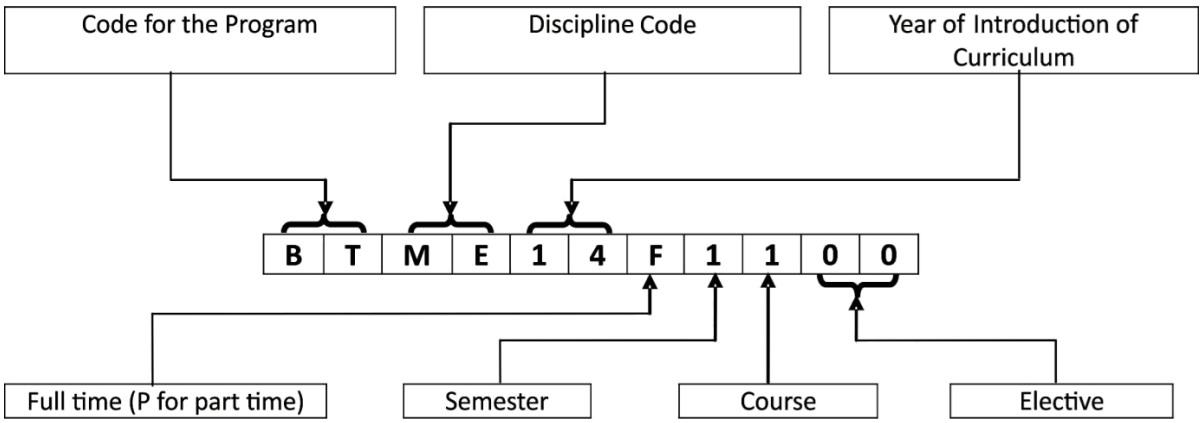
11.1. Grievance Cell:

For every program there will be one grievance cell. The composition of the grievance cell is as follows.

- The Registrar (Evaluation) - Ex-officio Chairman / Convener
- One Senior Faculty Member (other than those concerned with the evaluation of the course concerned) drawn from the school / department/discipline and/or from the sister schools / departments/sister disciplines – Member.
- One Senior Faculty Members / Subject Experts drawn from outside the University school / department – Member.

11.2. With regard to any specific case of ambiguity and unsolved problem, the decision of the Vice-Chancellor shall be final.

Course Numbering Scheme



List of Codes for Programs and Disciplines / Branch of Study

Program Code	Title of the Program	Discipline Code	Name of the Discipline / Branch of Study
BA	Bachelor of Arts	AE	Advanced Embedded Systems
BB	BBM (Bachelor of Business Management)	AI	Advanced Information Technology
BC	B.Com (Bachelor of Commerce)	AP	Advanced Power Electronics
BR	B. Arch (Bachelor of Architecture)	CA	Computer Aided Structural Engineering
BS	B Sc, BS (Bachelor of Science)	CE	Civil Engineering
BT	B.Tech (Bachelor of Technology)	CH	Chemistry
BP	Bachelor of Computer Applications	CO	Commerce
BL	LLB (Bachelor of Law)	CS	Computer Science and Engineering /
MA	Master of Arts	DE	Data Engineering and Cloud Computing
MB	MBA (Master of Business Administration)	EC	Electronics and Communication Engineering
MC	M.Com (Master of Commerce)	EN	English
MS	M.Sc / MS (Master of Science)	MD	Machine Design and Dynamics
MT	M Tech (Master of Technology)	ME	Mechanical Engineering
MC	Master of Computer Applications	EE	Electrical & Electronics Engineering

M. Tech. (VLSI and Embedded Systems) FULL-TIME

Eligibility: B.E./B. Tech. in ECE/TE/EEE/CSE/ISE/ Instrumentation Technology/ Medical Electronics/ Electrical and Electronics Engineering/ M Sc in Electronics with a minimum of 45% (40% in case of candidates belonging to SC and ST) marks in aggregate of any recognized university/institution or any other qualification recognized as equivalent there to.

Scheme of Instruction
2016-17

Sl No	Course Code	Title of the Course	HC/ SC	Credit Pattern				No. Hrs
				L	T	P	Total	
FIRST SEMESTER								
1	MTVS15F1100	Advanced Mathematics	HC	4	1	0	5	6
2	MTVS15F1200	Digital VLSI Design	HC	4	0	1	5	6
3	MTVS15F1300	Digital System Design	HC	4	0	1	5	6
4	MTVS15F1410	Embedded System Design	SC	4	1	0	5	6
	MTVS15F1420	Semiconductor Fabrication Technology						
5	MTVS15F1510	ASIC Design	SC	4	1	0	5	6
	MTVS15F1520	VLSI SOC Design		4	1	0		
		Total Credits					**25**	**30**
SECOND SEMESTER								
6	MTVS15F2100	Design of CMOS VLSI Circuits	HC	4	0	1	5	6
7	MTVS15F2200	Real Time Systems	HC	4	0	1	5	6
8	MTVS15F2310	Low Power VLSI Design	SC	4	1	0	5	6
	MTVS15F2320	VLSI for Signal Processing		4	1	0		
9	MTVS15F2410	High Speed VLSI Design	SC	4	1	0	5	6
	MTVS15F2420	VLSI Testing and Verification		4	1	0		
10	MTVS15F2510	MEMS and Nano-Electronics	SC	4	1	0	5	6
	MTVS15F2520	Advanced Computer Architecture		4	1	0		
		Total Credits					**25**	**30**

Sl No	Course Code	Title of the Course	HC/SC	Credit Pattern				No. Hrs
				L	T	P	Total	
THIRD SEMESTER								
11	MTVS15F3110	MSP430	SC	4	0	1	5	6
	MTVS15F3120	FPGA Based Embedded System Design		4	1	0		
	MTVS15F3130	Advanced Digital System Design		4	1	0		
	MTVS15F3140	CMOS RF Circuit Design		4	1	0		
	MTVS15F3150	Advances in VLSI Design		4	1	0		
12	MTVS15F3200	Seminar/Certification Program	HC	4	1	0	5	6
13	MTVS15F3300	Internship/Mini Project	HC	0	2	8	10	22
14	MTVS15F3400	Automotive Electronics Systems	OE	3	1	0	04	
		Total Credits					**24**	**38**
FOURTH SEMESTER								
15	MTVS15F4100	Dissertation	HC	0	2	20	22	40
		Total Credits					**22**	
	Total Credits for four Semesters						**96**	

Note: HC = Hard Core: SC= Soft Core;

Detailed Syllabus

Semester – I

Course Code	Course Title	Duration		L	T	P	C
MTVS15F1100	Advanced Mathematics	16 Weeks	HC	4	1	0	5

Prerequisites:

1. Basic knowledge of matrix mathematics and linear transformations.
2. Linear and parabolic partial differentiation and scalar wave equation in one space dimension.
3. Basics of Laplace transforms, Fourier transforms and Poisson equation by Fourier transform.
4. Simplex algorithm and nonlinear programming.

Course Objectives:

1. To understand the advanced concepts in Matrix theory and calculus.
2. To Study the numerical, analytical and logical problem solving using transform methods.
3. To learn applications of Poisson and Fourier transform methods.
4. To understand the concept of elliptic equation.
5. To study the various algorithms in linear and nonlinear programming.

Course Outcomes:

On completion of this course the student will be able to:

1. Identify and describe different techniques in solving Engineering problems using Matrix method.
2. Describe the Euler equation of first and higher order degree
3. Apply Laplace transform to one dimensional wave.
4. Analyse properties of harmonic functions
5. Present the concepts Two Phase and Big M techniques
6. Explain problem solving using Lagrange's multiplier method

Course Code	POS/ COs	PO 1	PO2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO 10	PO 11	PSO1	PSO2	PSO3
MTVS15F 1100	CO1	3	2	3	4					3			1	1	2
	CO2	3	3	2	1				2					2	1
	CO3	1	3	2	1					1					
	CO4	2	3	1	2										
	CO5	3	3	2	1				2					2	1
	CO6	3	3	2	1				2					2	1

Course Contents:

Unit 1:Matrix Theory, Calculus of Variations [16]

QR EL Decomposition – Eigen values using shifted QR algorithm- Singular Value EL Decomposition - Pseudo inverse- Least square approximations

Concept of Functional- Euler's equation – functional dependent on first and higher order derivatives – Functional on several dependent variables – Isoperimetric problems- Variation problems with moving boundaries.

Unit 2:Transform Methods **[16]**

Laplace transform methods for one dimensional wave equation – Displacements in a string – Longitudinal vibration of an elastic bar – Fourier Transform methods for one dimensional heat conduction problems in infinite and semi-infinite rod.

Unit 3: Elliptic Equation **[16]**

Laplace equation – Properties of harmonic functions – Fourier transforms methods for Laplace equations. Solution for Poisson equation by Fourier transforms method.

Unit 4:Linear and Non Linear Programming **[16]**

Simplex Algorithm- Two Phase and Big M techniques – Duality theory- Dual Simplex method. Non Linear Programming –Constrained external problems- Lagrange's multiplier method- Kuhn-Tucker conditions and solutions.Recent trends in the related areas from journals, Conference proceedings Book chapters.

References:

1. Richard Bronson, "**Schaum's Outlines of Theory and Problems of Matrix Operations**", McGraw-Hill, 1988.
2. Venkataraman M. K., "**Higher Engineering Mathematics**", National Publications Co., 1992.
3. Elsgolts, L., "**Differential Equations and Calculus of Variations**", Mir, 1977.
4. Sneddon, I.N., "**Elements of Partial Differential Equations**", Dover Publications, 2006.
5. Sankara Rao, K., "**Introduction to Partial Differential Equations**", Prentice – Hall of India,1995.
6. Taha H A, "**Operations Research - An Introduction**", McMilan Publishing co, 1982.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F1200	Digital VLSI Design	16 Weeks	HC	4	0	1	5

Prerequisites:

1. Working principle of MOS transistor theory and MOSFET characteristics.Static characteristics, transient response and propagation delay calculations of MOS inverters.
2. Basic principles of pass transistor circuits and dynamic CMOS characteristics.
3. Basics of volatile memory and non-volatile memory and low power CMOS logic circuits.
4. Knowledge on BiCMOS and BJT theory.
5. Concept of electrostatic discharge (ESD) and basics of latch up prevention and process variations.

Course Objectives:

1. To understand an overview of working principle of MOS transistor and MOS inverters.
2. To be acquainted with all the definitions associated with MOS inverters.
3. To understand dynamic logic circuits.
4. To get understand of semiconductor memory.
5. To study chip input output devices.

Course Outcomes:

On completion of this course the student will be able to:

1. Explain the working principle of MOS transistor and MOS inverters.
2. Define all the definitions associated with MOS inverters.
3. Analyse dynamic logic circuits.
4. Describe the semiconductor memory.
5. Explain chip input output devices.

Mapping of Course Outcomes with programme Outcomes

Course Code	POs/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
MTVS15F 1200	CO1	3	2		2		1	1			2		3		3	2
	CO2	3	3	3			1			2			2		3	2
	CO3	3	3				2			1			1		3	2
	CO4	3	3			2							1		3	2
	CO5	3	2		2		1	1			2		3		3	2

Course Contents:

Unit 1:MOS Transistor, MOS Inverters [16]

The Metal Oxide Semiconductor (MOS) Structure, the MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, and MOSFET Scaling and Small-Geometry Effects.

Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with type MOSFET Load, CMOS Inverter.

Unit 2: MOS Inverters (continued) [16]

Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, and Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, and Switching Power Dissipation of CMOS Inverters.

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.

Unit3: Semiconductor Memories [16]

Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM). Low-Power

CMOS Logic Circuits: Introduction, Overview of Power Consumption, Low-Power Design Through Voltage Scaling, Estimation and Optimization of Switching Activity, Reduction of Switched Capacitance, Adiabatic Logic Circuits.
BiCMOS Logic Circuits: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.

Unit 4:Chip Input and Output (I/O) Circuits [16]

Introduction, ESD Protection, Input Circuits, Output Circuits and L (di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.
Design for Manufacturability : Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling, Parametric Yield Estimation, Parametric Yield Maximization, Worst-Case Analysis, Performance Variability Minimization.
Recent trends in the related areas from journals, Conference proceedings Book chapters.

References:

1. Sung Mo Kang andYosufLeblebici, "**CMOS Digital Integrated Circuits: Analysis and Design**", Tata McGraw-Hill, Third Edition, 2003.
2. Neil Weste and K. Eshragian, "**Principles of CMOS VLSI Design: A System Perspective**", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F1300	Digital System Design	16 Weeks	HC	4	0	1	5

Prerequisites:

1. Knowledge on Digital system design, Boolean algebraic theorems and number systems.
2. Basics of sequential logic and memory types.
3. Principles of ICs, PLDs and interfacing memory.
4. Basic knowledge on I/O interfacing, serial transmission and design optimization.

Course Objectives:

1. Present an outline in to Introduction of Digital Design and Methodology involved in Digital System Design.
2. Illustrate the different components and functions related to design of Combinational circuits.
3. Illustrate with examples the various operations and types related to Number Basics.
4. Illustrate the different components and methodology related to design of Sequential circuits.
5. Provide an understanding in to the concepts and types of memories and design of memory circuits.
   Provide an explanation in to different Digital Design Implementation Fabrics.
6. Provide an Understanding to concepts related to processor basics.

Course Outcomes:

1. Distinguish between Digital and Embedded Systems and to have an understanding of the Binary representation, elements and Design Methodology of a Digital System.
2. Distinguish between Combinational and Sequential Basics and to demonstrate the knowledge of Number basics.
3. Analyse various types of implementation fabrics.
4. Apply knowledge related to processor basics.
5. Define and describe digital design flows for system design and to recognize the trade-offs involved in different approaches.

Mapping of Course Outcomes with programme Outcomes

Course Code	POS/ COs	PO 1	PO2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
MTVS 15F1 300	CO1	4	4	3	3	2							1	1		2
	CO2	1	4	3	3	2							2	1		2
	CO3	4	3	4	2	2					1		1	1		2
	CO4	1	3	4		2							1	1		2
	CO5	4	4	3	3	2							1	1		2

Course Contents:

Unit 1:Introduction and Methodology [16]

Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.

Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers. Combinational Basics: Boolean Functions and Boolean algebra, Binary Coding, Combinational components and circuits, Verification of combinational circuits.

Unit 2:Sequential Basics [16]

Storage elements, Counters, Sequential Data paths and Control, Clocked Synchronous Timing Methodology. Memories: Concepts, Memory Types, Error Detection and Correction.

Unit 3:Implementation Fabrics [16]

ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal integrity. Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory.

Unit 4:I/O interfacing [16]

I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software. Accelerators: Concepts, case study, Verification of accelerators.

Design Methodology: Design flow, Design optimization, Design for test.

References:

1. Peter J. Ashenden, "**Digital Design: An Embedded Systems Approach Using VERILOG**", Elesvier, 2010.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F1410	Embedded Systems Design	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Concept of Embedded systems and its design optimization.
2. Knowledge on architecture of embedded systems and embedded microcontroller cores.
3. Working principle of interfacing subsystems and external systems and DSP.
4. Concepts of real time programming and RTOS.

Course Objectives:

1. Understand how to design an embedded system.
2. To know how to partition a system to hardware and software parts efficiently.
3. To know Hardware/software Co-design concepts.
4. To understand the issues and technologies involved in designing real-time and hardware-resource constrained systems.
5. To be acquainted with understanding and to make decisions about general purpose computing solutions vs. specialized hardware solutions using FPGA's, CPLD.
6. To understand interfacing system for profiling system performance.
7. To be acquainted with the system architectures for optimum performance.

Course Outcomes:

On completion of this course the students will be able to:

1. Design embedded system architectures for various applications.
2. Implement, Identify, formulate, and solve engineering problems.
3. Function on multidisciplinary teams
4. Implement embedded microcontroller cores.
5. Analyze and Apply knowledge of RTOS for various applications.
6. Demonstrate sub system interfacing with external system

Mapping of Course Outcomes with Programme Outcomes

Course Code	POS/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
MTVS15 F1410	CO1	3	3	3		2				2	3		3	2	3	2
	CO2	3	3	3		2				2	3		3	2	3	2
	CO3	3	3	3		2				2	3		3	2	3	2
	CO4	3	3	3		2				2	3		3	2	3	2
	CO5	3	3	3		2				2	3		3	2	3	2
	CO6	3	3	3		2				2	3		3	2	3	2

Course Contents:

Unit 1:Introduction **[16]**

Overview of embedded systems, embedded system design challenges, common design metrics

and optimizing.
Survey of different embedded system design technologies & trade-offs.

Unit 2:Embedded systems **[16]**
Embedded microcontroller cores, embedded memories, Examples of embedded systems. Architecture for embedded system,
High performance processors – strong ARM processors, programming, interrupt structure, I/O architecture.

Unit 3:Technological aspects of embedded systems **[16]**
Interfacing between analog and digital blocks, signal conditioning, Digital signal processing, Sub-system interfacing, interfacing with external systems.

Unit 4:Software aspects of embedded systems **[16]**
Real time programming languages and operating systems for embedded systems – RTOS requirements, kernel types, scheduling, context switching, latency, inter-task communication and synchronization, Case studies.

References:

1. Jack Ganssle, "**The Art of Designing Embedded Systems**", Elsevier, 1999.J.W. Valvano, "**Embedded Microcomputer System: Real Time Interfacing**", Brooks/Cole, 2000.
2. David Simon, "An Embedded Software Primer", Addison Wesley, 2000.
3. H. Kopetz, "**Real-time Systems**", Kluwer, 1997
4. R. Gupta, "**Co-synthesis of Hardware and Software for Embedded Systems**", Kluwer 1995.
5. Gomaa, "**Software Design Methods for Concurrent and Real-time Systems**", Addison-Wesley, 1993.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F1420	Semiconductor Fabrication Technology	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Knowledge on Modern CMOS technology, properties of silicon wafers and insulators technology.
2. Concept of lithography and fabrication processing steps.
3. Knowledge of ion implantation and diffusion techniques.
4. Concept of sub-micron device and backend technologies.

Course Objectives:

1. Understand crystal growth and wafer preparation.
2. Study various types of lithography.

3. Learn Dielectric and polysilicon film deposition.
4. Understand the concept of VLSI process Integration.
5. Learn Metallization in IC fabrication.
6. Study IC process technology andpackaging.

Course Outcomes:

On completion of this course the student will be able to:

1. Describe different techniques crystal growth and wafer preparation of VLSI technology
2. Describe the concept of lithography and its types in VLSI technology.
3. Present various types of dielectric and polysilicon film deposit
4. Analyse process of metallization in VLSI technology
5. Present the process of packing

Mapping of Course Outcomes with Programme Outcomes

Course Code	POS/ COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
MTVS15 F1420	**CO1**	**3**	**3**	**3**		**2**				**2**	**3**		**3**	**2**	**3**	**2**
	CO2	**3**	**3**	**3**		**2**				**2**	**3**		**3**	**2**	**3**	**2**
	CO3	**3**	**3**	**3**		**2**				**2**	**3**		**3**	**2**	**3**	**2**
	CO4	**3**	**3**	**2**		**2**				**2**	**3**		**3**	**2**	**2**	**2**
	CO5	**2**	**2**	**2**		**2**				**2**	**3**		**3**	**2**	**3**	**2**

Course Contents:

Unit 1: Introduction **[16]**

Introduction and Historical Perspective, Moors Law, Integrated Circuits and the Planar Process. Modern CMOS Technology, Crystal Growth, Wafer Fabrication and Basic Properties of Silicon Wafers, Silicon on Insulators technology.

Unit 2: Semiconductor Manufacturing **[16]**

Clean Rooms, Wafer Cleaning and Guttering, Lithography: Thermal Oxidation and the Si/SiO_2 Interface.

Unit 3: Diffusion and implantation **[16]**

Dopant Diffusion, Ion Implantation, Thin Film Deposition, Etching.

Unit 4: Backend Technology **[16]**

Introduction to deep submicron device technology, Lithography, strained silicon, Atomic layer deposition, HI-K dielectrics, Finfet fabrication technology.

References:

1. James D. Plummer, Michael D. Deal and Peter B. Griffin, "**Silicon VLSI Technology: Fundamentals, Practice and Modelling**" Prentice Hall Electronics and VLSI Series , 2001.

2. Stephen A. Campbell "**The Science and Engineering of Microelectronic Fabrication**" Oxford University Press, 2001.
3. S. Wolf and R. N. Tauber, "**Silicon Processing for the VLSI Era**",(Volume 1- "**Process Technology**", Volume 2 – "**Process Integration**", Volume 3 – "**The Submicron MOSFET**", Vol. 4–"***Deep-Submicron Process Technology****": 2002)*, Lattice Press, Sunset Beach, California.
4. Gary S. May and Costas J. Spanos, "**Semiconductor Manufacturing and Process Control**" IEEE, Wiley-Interscience, 2006.
5. Jose Pineda de Gyvez and Dhiraj K. Pradhan, "Int**egrated Circuit Manufacturability – The Art of Process and Design Integration**" IEEE Press, 2006.
6. S. M. Sze, "**VLSI Technology**", McGraw-Hill, Second Edition, 2003.
7. S.K. Ghandhi, "**VLSI Fabrication Principles**", John Wiley Inc., New York, , Second Edition, 1994.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F1510	ASIC Design	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Principles of different ASIC designs and design flow of FPGA.
2. Concept of data logic cells and library design parameters of ASIC.
3. Programming concepts of VHDL/ Verilog and basics of low level design language.
4. Basic knowledge of floor planning, placement and routing.

Course Objectives:

1. To understand full custom, semicustom ASICS.
2. To Study the various Data logic cells.
3. To learn about ASIC library design.
4. To know the concept schematic entry hierarchical design and cell library.
5. To understand programmable ASIC, and simulation examples.
6. To study ASIC construction and floor planning.

Course Outcomes:

On completion of this course the student will be able to:

1. Describe full custom, semicustom ASICS.
2. Analyse various Data logic cells
3. Explain ASIC library design.
4. Describe concept schematic entry hierarchical design and cell library
5. Know the concept of programmable ASIC, and simulation examples
6. Explain ASIC construction and floor planning

Mapping of Course Outcomes with programme Outcomes

Cours e Code	POS / COs	PO 1	P0 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	P O 1 0	P O1 1	P O 1 2	PS O 1	PS O 2	PS O 3
MTVS15F1 510	CO1		2	1		3								3	1	2
	CO2	2	1		2	3								1	3	2
	CO3	1		2		3								2	3	1
	CO4		2	1		3								3	1	2
	CO5	2	1		2	3								1	3	2
	CO6	1		2		3								2	3	1

Course Contents:

Note: All Designs Will Be Based On VHDL/VERILOG.

Unit 1: Introduction [16]

Full Custom with ASIC, Semi-custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channelless gate array, structured get array, Programmable logic device, FPGA design flow, SIC cell libraries.

Data Logic Cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers.

Unit 2: ASIC Library Design [16]

Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum number of stages, library cell design.

Low-Level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry or ASIC'S, connections, vectored instances and buses, Edit in place attributes, Net list, screener, Back annotation.

Unit 3: Programmable ASIC [16]

Programmable ASIC logic cell, ASIC I/O cell.

A Brief Introduction to Low Level Design Language: an introduction to EDIF, PLA Tools, and an introduction to CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation, examples.

Unit 4:ASIC Construction Floor Planning and Placement and Routing [16]

Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

Recent trends in the related areas from journals, Conference proceedings Book chapters.

References:

1. M.J.S .Smith, - "**Application - Specific Integrated Circuits**" – Pearson Education, 2003.
2. Jose E.France, YannisTsividis, "**Design of Analog-Digital VLSICircuits forTelecommunication and signal processing**", Prentice Hall, 1994.
3. MalcolmR.Haskard; Lan. C. May, "**Analog VLSI Design – NMOSand CMOS**", Prentice Hall, 1998.

4. Mohammed Ismail and Terri Fiez, "**Analog VLSI Signal andInformationProcessing**", McGraw Hill, 1994.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F1520	VLSI SOCDesign	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Basics of SoC design and system architecture.
2. Concepts of interconnect architecture and bus architecture of Soc.
3. Principles of memory design and cache architecture.
4. Basic knowledge of ASIC design flow and FPGA design flow.

Course Objectives:

1. Provide a comprehensive introduction to the ASIC and SoC technology.
2. Provide theoretical and practical aspects of ASIC and SoC design.
3. Introduce ASIC design, ASIC library design and Programmable ASIC.
4. Give an overview to SoC design, its challenges and Design flow.
5. To understand the memory design concepts in processors.
6. To understand ASIC design flow using semi/full /standard cells.

Course Outcomes:

On completion of this course the students will be able to:

1. Design processors keeping area, power and speed as constraints and to Deepen CMOS VLSI design knowledge
2. Design full custom/ semicustom/ standard cells for ASIC
3. Implement network on chip technologies
4. Analyse memories using reconfigurable architectures for rapid prototyping
5. Analyse system on chip and board based systems

Mapping of Course Outcomes with programme Outcomes

Course Code	POS / COs	PO 1	P0 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
MTVS15F1520	**CO1**		**2**	**1**		**3**								**3**	**1**	**2**
	CO2	**2**	**1**		**2**	**3**								**1**	**3**	**2**
	CO3	**1**		**2**		**3**								**2**	**3**	**1**
	CO4		**2**	**1**		**3**								**3**	**1**	**2**
	CO5	**2**	**1**		**2**	**3**								**1**	**3**	**2**

Course Contents:

Unit 1:System Approach and Chip Basics **[16]**

System Architecture, Components of the System, Hardware and Software. An approach for SoC Design, System Architecture and Complexity. Chip Basics. Cycle Time, Die Area and Cost, Ideal and Practical Scaling, Power, Area–Time–Power Trade-Offs in Processor Design, Reliability, Configurability.

Unit 2:Processors and Interconnects [16]

Processor Selection for SoC, Basic Concepts in Processor Architecture, Instruction Handling, and Buffers, Minimizing Pipeline Delays, Branches. Vector, Very Long Instruction Word (VLIW), and Superscalar with case studies. Interconnect architectures for SoC. Bus architecture. Network on Chip topologies. Routing, Switching and Flow Control in NoCs.

Unit 3:Memory Design [16]

System-on-Chip and Board-Based Systems – Scratchpads and Cache Memory, Basic Notions, Cache Organization, Cache Data, Write Policies, Strategies for Line Replacement at Miss Time, Other Types of Cache, Split I- and D-Caches and the Effect of Code Density, Multilevel Caches, Virtual-to-Real Translation, SoC (On-Die) Memory Systems, Board-based (Off-Die) Memory Systems, Simple DRAM and the Memory Array, Models of Simple Processor–Memory Interaction.

Unit 4:ASIC Design [16]

Full/Semi Custom with ASIC, Standard Cell based ASIC, Gate array based ASIC, Programmable logic device, FPGA design flow, ASIC cell libraries. ASIC Library Design, Logical effort and library cell design. Low-Level Design Entry, Schematic Entry, Hierarchical design, the cell library, connections, vectored instances and buses, Edit in place attributes, Net list, screener, back annotation.

References:

1. Micheal J Flynn and Wayne Luk,"**Computer System Design: System-on-Chip**," Wiley, First Edition, 2011.
2. Sudeep Pasricha and NikilDutt,"**On-Chip Communication Architectures: System on Chip Interconnect**", Morgan Kaufmann, 2008.
3. Michael Keating, Pierre Bricaud, "**Reuse Methodology manual for System on chip designs**", Kluwer academic Publishers, 2nd edition-2008.
4. M.J.S .Smith, "**Application Specific Integrated Circuits**", Pearson Education, 2003.
5. Rao R. Tummala, Madhavan Swaminathan, "**Introduction to system on package sop-Miniaturization of the Entire System**", McGraw-Hill-2008.
6. James K. Peckol, "**Embedded Systems: A Contemporary Design Tool**", WILEY Student Edition, 2007.
7. Ahmed Amine Jeraya, Wayne Wolf, "**Multiprocessor System On chip**", Morgan Kauffmann, 2005.
8. Sung- Mo Kang, Yusuf Leblebici, "**CMOS Digital Integrated Circuits**", Tata McGraw-hill, 3rd Edition, 2012.

Semester – II

Course Code	Course Title	Duration		L	T	P	C
MTVS15F2100	Design of CMOS VLSI Circuits	16 Weeks	HC	4	0	1	5

Prerequisites:

1. Basics of MOS devices and its characteristics.
2. Concepts of single stage amplifiers and frequency response of amplifiers.
3. Knowledge on differential amplifiers, Operational amplifiers and current mirrors.
4. Basic knowledge on DAC and ADC architectures and phase locked loops.

Course Objectives:

1. To understand the basics and operation of MOS devices.
2. To analyse and understand analog CMOS integrated circuits.
3. To analyse and design single stage MOS amplifier circuits.
4. To understand the basic operation of differential amplifier and op-amps.

Course Outcomes:

On completion of this course the student will be able to:

1. Design single stage, differential and current mirror
2. Analyse the stability, feedback in amplifiers, op-amps
3. Design oscillators and PLL.
4. Design ADCs and DACs

Mapping of Course Outcomes with Program Outcomes

Course Code	POs / COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PSO 1	PSO 2	PSO 3
	CO1	3	2	3	1								2	1	3
	CO2	3	3	2	1								1	2	3
	CO3	2	2	3	2								3	1	
	CO4	2	1	2	1								2	3	

Course Contents:

Unit 1:Basic MOS Device Physics **[16]**

General considerations, MOS I/V Characteristics, second order effects, MOS device models. Single stage Amplifier:CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models**.**

Frequency response of CS stage:source follower, Common gate stage, Cascade stage and Difference pair. Noise in CS stage, C- G stage, source follower, cascade stage, differential pair.

Unit 2: Differential Amplifiers & Current Mirrors **[16]**

Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. Basic current mirrors, Cascade mirrors, active current mirrors.

Operational Amplifiers: One Stage OP-Amp, Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, Power Supply Rejection, Noise in Op Amps.

Unit 3: Oscillators and Phase Locked Loops **[16]**

Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications. Band gap References and Switched capacitor Circuits: General Considerations, Supply Independent biasing, PTAT Current Generation, Constant Gm Biasing, Sampling Switches, and Switched Capacitor Amplifiers.

Unit 4: Data Converter Architectures **[16]**

DAC & ADC Specifications, Resistor String DAC, R-2R Ladder Network, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.

References:

1. BehzadRazavi, “Design of Analog CMOS Integrated Circuits”, TMH, 2007.
2. Philip Allen and Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University, Press, 2011.
3. R. Jacaob Baker, Harry W Li and David E Boyce, “CMOS Circuit Design, Layout, Stimulation”, CMOS Circuit PHI Edn, 2005.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F2200	Real Time Systems	16 Weeks	HC	4	0	1	5

Prerequisites:

1. Concepts of real time systems and clock synchronization.
2. Basics of task management and task scheduling.
3. Knowledge on RTOS and memory management.
4. Basic knowledge on performance metrics and RTOS tools.

Course Objectives:

1. Understand and Analyse Real Time Systems.
2. Know the Importance of real time constraints and synchronization issues.
3. Introduce concepts of RTOS and resource management.
4. Study multitasking and concurrency.
5. Know RTOS tools and case studies.

Course Outcomes:

On completion of this course the students will be able to:

1. Understand the basics and importance of real-time systems.
2. Generate a high-level analysis document based on requirements specifications.
3. Generate a high-level design document based on analysis documentation
4. Generate a test plan based on requirements specification
5. Generate a validation plan based on all documentation
6. Understand basic multi-task scheduling algorithms for periodic, a periodic, and sporadic tasks as well as understand the impact of the latter two on scheduling
7. Understand capabilities of at least one commercial off-the-shelf R-T kernel
8. Participate in a team design project, utilizing varying skill sets of members.

Mapping of Course Outcomes with Program Outcomes

Course Code	POs/ COs	PO1	PO 2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO 10	PO 11	PSO 1	PSO 2	PSO 3
MTVS15F2200	CO1	3	2	3	1								2	1	3
	CO2	3	3	2	1								1	2	3
	CO3	2	2	3	2								3	1	
	CO4	2	1	2	1								2	3	
	CO5	3	2	3	1								2	1	3
	CO6	2	1	2	1								2	3	
	CO7	2	1	2	1								2	3	
	CO8	1	1	1	1						1		2	2	2

Course Contents:

UNIT 1: Introduction to Real Time Systems [16]

Basic Real-Time Concepts, Hardware Considerations, Clock Synchronization.

UNIT 2:Tasks and Task Scheduling [16]

Task classes, Characterizing RTS and Tasks, Task assignment and Scheduling, Task management, Scheduler and Real-Time Clock Interrupt Handler, Resource Control (IOSS), OS services, I/O subsystems, Network OS.

UNIT 3:RTOS [16]

Introduction, Real Time Multi-tasking Operating Systems, Real-Time Kernels, Scheduling Strategies, Priority Structures, Theoretical Foundations of Real-Time Operating Systems, and Intertask Communication and Synchronization, Memory Management. Design of Real Time Systems: General Introduction**,** Design Analysis.

UNIT4:RTOS Issues and Tools [16]

Performance Metrics, Synchronization issues, Embedded Linux internals, RTOS Tools- mucos, VxWorks- case studies on these tools, POSIX Thread Programming.

References:

1. Philip A. Laplante, "**Real Time System Design and Analysis**", Third edition, Wiley India Edition, 2011.
2. C.M. Krishna and Kang G. Shin, "**Real Time Systems**", MGH, 1997.
3. Staurt Bennett, "**Real Time Computer Control**", Second Edition, Pearson, 2002.Raj Kamal, "**Embedded Systems Architecture, Programming and Design**", Second Edition, TMH, 2003.
4. Jane W. S. Liu, "**Real Time Systems**", Pearson Education, 2000.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F2310	Low Power VLSI Design	15 Weeks	SC	4	1	0	5

Prerequisites:

1. Concepts of low power VLSI design and scaling technologies involved.
2. Knowledge on simulation programming with integrated circuits and probabilistic power analysis.
3. Basics of design parameters of low power circuits and low power architecture.
4. Knowledge on clock distribution and architectural level methodologies.

Course Objectives:

1. To understand different sources of power dissipation in CMOS & MIS structure.
2. To understand the different types of low power adders and multipliers.
3. To focus on synthesis of different level low power transforms.
4. To understand the various energy recovery techniques used in low power design.

Course Outcomes:

On completion of this course the student will be able to:

1. Analyse different source of power dissipation and the factors involved.
2. Understand the different techniques involved in low power adders and multipliers.
3. Understandings of the impact of various low powers transform.
4. Identify and analyse the different techniques involved in low power SRA

Mapping of Course Outcomes with Program Outcomes:

Cour se Code	POs/ COs	P O 1	P O2	P O3	P O4	P O5	P O6	P 7	P O8	P O9	P O 1 0	P O 1 1	P O 1 2	PS O1	PS O 2	PS O3
MTVS15F2310	CO1	3	3							3	3	2				
	CO2	3	2	3						3	3	3		3		3
	CO3	3	3							3	2	3				
	CO4	3	3							2	1	3		3		

Course Contents:

Unit 1: Introduction **[16]**

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Unit 2: Power estimation, Simulation Power analysis **[16]**

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Unit 3: Low Power Design Circuit level **[16]**

Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Unit 4:Low power Clock Distribution **[16]**

Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip& package co design of clock network.

Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

References:

1. Kaushik Roy, Sharat Prasad, "**Low-Power CMOS VLSI Circuit Design**" Wiley, 2000.
2. Gary K. Yeap, "**Practical Low Power Digital VLSI Design**", KAP, 2002.
3. Rabaey, Pedram, "**Low Power Design Methodologies**" Kluwer Academic, 1997.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F2320	VLSI for Signal Processing	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Concepts of DSP systems and its architecture.
2. Basic knowledge on FIR digital filters.
3. Concepts of retiming and systolic architecture.
4. Knowledge of recursive and adaptive filters.
5. Basics on algorithms used in fast convolution method.

Course Objectives:

1. To understand the basic concepts of DSP algorithms.
2. To analyze the various pipelining and parallel processing techniques.
3. To analyze the retiming and unfolding algorithms for various DSP applications.

Course Outcomes:

On completion of this course the student will be able to:

1. Apply DSP algorithms on to the IC technology
2. Analyze the concept of pipelining and other processing for DSP applications

Mapping of Course Outcomes with programme Outcomes

Course Code	POS / COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
MTVS15F 2320	CO1	1		2			3							3	1	2
	CO2	1	3				3							2	1	3
	CO3	1		2			3							3	2	1

Course Contents:

Unit 1: Introduction to DSP systems [16]

Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.

Iteration Bounds: Data flow graph Representations, loop bound and Iteration bound, Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.

Pipelining and parallel processing, pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.

Unit 2: Retiming [16]

Definition and Properties, Solving Systems of Inequalities, Retiming Techniques, Unfolding an Algorithm for Unfolding, Properties of Unfolding, and Critical path, Unfolding and Retiming, Application of Unfolding. Systolic architecture design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays**.**

Unit 3:Fast convolution [16]

Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic Convolution Design of fast convolution Algorithmby Inspection.

Unit 4:Pipelined and Parallel recursive and adaptive filter [16]

Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using

Pipe lining and parallel processing, pipelined Adaptive digital filter.

References:

1. KeshabK.Parthi, "**VLSI Digital Signal Processing systems, Design and Implementation**", Wiley, Inter Science, 1999.
2. Mohammed Isamail and Terri Fiez, "**Analog VLSI Signal and Information Processing**", Mc Graw-Hill, 1994.
3. S.Y. Kung, H.J. White House, T. Kailath, "**VLSI and Modern Signal Processing**", Prentice Hall, 1985.
4. Jose E. France, YannisTsividis, "**Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing**", Prentice Hall, 1994.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F2410	High Speed VLSI Design	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Knowledge on high speed digital design and its issues.
2. Concept of noise and power supply network.
3. Principles of synchronization and timing convention.
4. Basic knowledge on clocked and no clocked logics and latching strategies.

Course Objectives:

1. Introduce the concept of high speed digital circuits.
2. Understand the power distribution and noise sources in VLSI circuits.
3. Understand the importance of timing analysis in high speed VLSI circuits.
4. Introduce the concept of latch and clock driven logic circuits for high speed VLSI circuits.

Course Outcomes:

On completion of this course the student will be able to:

1. Identify and analyse the sources of noise in VLSI circuits.
2. Describe the Signalling modes for transmission lines in VLSI circuits
3. Perform the timing analysis for VLSI Circuits.
4. Design the clocked and non-clocked logic circuits
5. Design various latch based digital circuits

Mapping of Course Outcomes with Program Outcomes:

Course Code	POs/ COs	PO1	PO2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
MTVS15F2410	CO1	3	3							3	3	2				
	CO2	3	2	3						3	3	3		3		3
	CO3	3	3							3	2	3				
	CO4	3	3							2	1	3		3		
	CO5	3	3							2	1	3		3		

Course Contents:

Unit 1: Introduction to High Speed Digital Design [16]

Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power. Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.

Unit 2: Power distribution and Noise [16]

Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors and symbiotic bypass capacitors. Power supply isolation. Noise sources in digital systems, power supply noise, crosstalk and inter symbol interference.

Signaling convention and circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.

Unit 3: Timing Convention and Synchronization [16]

Timing fundamentals, timing properties of clocked storage elements, signals and events, open loop timing, level sensitive clocking, pipeline timing, closed loop timing, clock distribution, synchronization failure and meta-stability, clock distribution, clock skew and methods to reduce clock skew, controlling crosstalk in clock lines, delay adjustments, clock oscillators and clock jitter - PLL and DLL based clock aligners.

Unit 4: Clocked & Non-Clocked Logics [16]

Single-Rail Domino Logic, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families.

Latching Strategies: Basic Latch Design, and Latching single-ended logic and Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques.

References:

1. William S. Dally & John W. Poulton, "**Digital Systems Engineering**", *Cambridge University Press*, 1998.
2. Kerry Bernstein &ET. Al., "**High Speed CMOS Design Styles**", Kluwer, 1999.
3. Howard Johnson & Martin Graham, "**High Speed Digital Design**" A Handbook of Black Magic, *Prentice Hall PTR*, 1993.
4. Masakazu Shoji, "**High Speed Digital Circuits**", *Addison Wesley Publishing Company*, 1996.
5. Jan M, Rabaey, et al, "**Digital Integrated Circuits**", A Design Perspective, *Pearson*, 2003.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F2420	VLSI Testing and Verification	16Weeks	SC	4	1	0	5

Prerequisites:

1. Knowledge on testing concepts and test generation for combinational logic circuits.
2. Concepts of generating test sequence for sequential circuits.
3. Basic knowledge on design verification, verification tools and verifying strategies.

Course Objectives:

1. To understand the Concepts of Verification Techniques and Tools.
2. To study the concepts of Verification Plan, Stimulus and Response.
3. To understand the concepts of Architecting Test benches and System Verilog.

Course Outcomes:

On completion of this course the student will be able to:

1. Understand and apply timing issues in multiple contexts and design the circuit
2. Design digital systems using modern design tools

Mapping of Course Outcomes with Program Outcomes:

Course Code	POs / COs	PO1	PO2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
	CO1	3	3					2		3	3	2				
	CO2	3	2	3						3	3	3		3		3

Course Contents:

Unit 1:Introduction to Testing **[16]**

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing. Faults in Digital Circuits: Failures and Faults, Modeling of Faults, Temporary Faults.

Test Generation for Combinational Logic Circuits:Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits.

Unit 2:Design of Testable Sequential Circuits **[16]**

Controllability and Observability, Ad Hoc Design Rules for Improving Testability, Design of Diagnosable Sequential Circuits, and The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access Scan Technique, Partial Scan, and Testable Sequential Circuit Design Using Nonscan Techniques, CrossCheck, and Boundary Scan.

Built-In Self-Test: Test Pattern Generation for BIST, Output Response Analysis, Circular BIST, BIST Architectures.

Unit 3:Importance of Design Verification **[16]**

What is verification? What is attest bench? The importance of verification, Re convergence model, Formal verification, Equivalence checking, Model checking, Functional verification.
Verification Tools: Linting tools: Limitations of linting tools, linting verilog source code, linting VHDL source code, linting OpenVera and e-source code, code reviews. Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.
The verification plan: The role of verification plan, specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses.

Unit 4: Static Timing Verification **[16]**

Concept of static timing analysis. Cross talk and noise. Limitations of STA. slew of a wave form, Skew between the signals, Timing arcs and unateness, Min and Max timing paths, clock domains, operating conditions, critical path analysis, false paths, Timing models.
Physical Design Verification: Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, Crosstalk and Noise**:** Cross talk glitch analysis, crosstalk delay analysis, timing verification.

References:

1. P. K. Lala, "**Digital Circuit Testing and Testability**", Academic Press, 1997.
2. M.L. Bushnell and V.D. Agrawal, "**Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits**", Kluwar Academic Publishers, 2000.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "**Digital Systems and Testable Design**", Jaico Publishing House, 2002.
4. JanickBergeron, "**Writing test benches: functional verification of HDL models**", second edition, Kluwer Academic Publishers, 2003.
5. JayaramBhasker,RakeshChadha, "**Static Timing Analysis for Nanometer Designs**" A practical approach, Springer publications, 2009.
6. PrakashRashinkar, PeterPaterson,Leena Singh "**System on a Chip Verification**", Kulwer Publications, 2001.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F2510	MEMS andNano-Electronics	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Knowledge on MEMS technology and its fabrication techniques.
2. Concepts of Nano electronics, Nano structures and Nano particles.
3. Basic knowledge on application of MEMS technology.

Course Objectives:

1. Understand the basic knowledge of emerging micro/nano electronic devices.
2. Understand the properties, synthesis methods and various characterization techniques of the micro/nano materials.
3. Study and enable the student to incorporate his/her own innovative ideas, which impact the industry roadmaps.
4. Know the knowledge of packaging, testing and applications.
5. Know the properties of nano particles.

Course Outcomes:

On completion of the course the students will be able to:

1. Design Digital micro mirrors, optical circuits and sensors.
2. Work effectively, independently, and in multi-person teams.
3. Implement wireless MEMS, RF MEMS
4. Analyse the properties of inorganicNano structures.
5. Analyse the challenges in MEMS.

Mapping of Course Outcomes with programme Outcomes

Course Code	POS / COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
MTV S15F 2510	CO1	1		2		3		3					4	1		2
	CO2	1			2	3		4		3				1		2
	CO3	1	1	2		3	4	2						1		2
	CO4	1		3			2					3	4	1		2
	CO5	1		3			2					3	4	1		2

Course Contents:

Unit 1 :Overview of MEMS **[16]**

What are MEMS? Why MEMS? How are MEMS made? History of MEMS, Fundamental Properties, Advantages and Challenges of MEMS, Future of MEMS. Fabrication Technologies and Characterization Methods.

Unit 2: **Packaging, Testing And Applications** **[16]**

Packaging and Assembly, Power for MEMS, Testing, Few Applications: Digital Micro Mirrors, Optical Circuits, Sensors, Inkjet Printing, Wireless MEMS, RF-MEMS etc.

Unit 3:Overview of Nanoelectronics **[16]**

Overview of nanoscience and engineering, Moore's law and continued miniaturization, Classification of Nano structures, Summary of Electronic properties of atoms and solids, Effects of nanometer length scale, Top down processes, Bottom up processes.

Unit-4:Properties of Individual Nanoparticles **[16]**

Properties of Individual Nano Particles, Generic Methodologies for Characterization, Inorganic Semiconductor Nanostructures, Emerging device technologies-Resonant Tunneling Devices, Single Electron Devices, Quantum Cellular Automata, Spintronics, Carbon Nanotubes, NEMS, and Nonmagnetic etc.

References:

1. Thomas M Adams et al. "**Introductory MEMS- Fabrication and Applications**" Springer, 2010.
2. Tai Ran Hsu et al., "**MEMS and Microsystems, Design & Manufacture**", TMH2002.
3. Mohammed had-el-hak et al., "**MEMS Introduction & Fundamentals**", CRC Press, 2007.
4. Robert Kelsall et al., "**NanoScale Science and Technology**", Wiley, 2005
5. Charles.P.Poole et al.,"**Introduction to Nanotechnology**" John Wiley,2006.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F2520	Advanced Computer Architecture	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Concepts of computer design, pipelining and instruction level parallelism.
2. Knowledge on design of memory hierarchy and real faults in a system.
3. Basic knowledge on very long instruction word and EPIC.
4. Concepts of multiprocessors and interprocessor communication.
5. Concepts of computer arithmetic.

Course Objectives:

1. Introduce the fundamentals of computer design.
2. Understand the quantitative principles of computer design and their performance.
3. Understanding the concepts of instruction level parallelism.
4. Introduce the fundamentals of advanced memory hierarchy.
5. Introduce the basics of VLIW processors.
6. Understand the concepts of multiprocessors and inter process communication.
7. Study of computer arithmetic blocks.

Course outcomes:

On completion of this course the student will be able to:

1. Analyse the importance of power and performance for given computer architecture.
2. Identifying the pitfalls and fallacies for the performance in the computer architecture.
3. Describe the instruction level parallelism and its importance with respect to performance and power dissipation in computer architecture
4. Calculate the performance of I/O devices
5. Designing the efficient hardware and software for the VLIW processors.

6. Designing the efficient arithmetic components for computer architecture.

Mapping of Course Outcomes with Program Outcomes

Course Code	POS/ COs	PO1	P2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
MTVS15F2520	CO1	3		1				3					3	3	2	2
	CO2	2		2				3					3	3	2	1
	CO3	2		2				3					3	3	2	2
	CO4			3				3					3			2
	CO5	2		2				3					3	3	2	2
	CO6	2		2				3					3	3	2	2

Course Contents:

Unit 1:Introduction and Review of Fundamentals of Computer Design [16]

Introduction; Classes computers, Defining computer architecture, Trends in Technology, Trends in power in Integrated Circuits, Trends in cost, Dependability, Measuring, reporting and summarizing Performance, Quantitative Principles of computer design, Performance and Price-Performance; Fallacies and pitfalls; Case studies.

Some topics in Pipelining, Instruction –Level Parallelism, Its Exploitation and Limits on ILP:Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls with respect to pipelining, Basic concepts and challenges of ILP, Case study of Pentium 4, Fallacies and pitfalls. Introduction to limits in ILP, Performance and efficiency in advanced multiple-issue processors.

Unit 2:Memory Hierarchy Design, Storage Systems [16]

Review of basic concepts, Cross cutting issues in the design of memory hierarchies, Case study of AMD Opteron memory hierarchy, Fallacies and pitfalls in the design of memory hierarchies, Introduction to Storage Systems, Advanced topics in disk storage.

Definition and examples of real faults and failures: I/O performance, reliability measures, and benchmarks; Queuing theory; Crosscutting Issues, Designing and evaluating an I/O system – The Internet archive cluster; Case study of NetAA FAS6000 filer; Fallacies and pitfalls.

Unit 3:Hardware and Software for VLIW and EPIC Introduction [16]

Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop-Level Parallelism, Scheduling and Structuring Code for Parallelism, Hardware Support for Exposing Parallelism: Predicated Instructions, Hardware Support for Compiler Speculation, The Intel IA-64 Architecture and Itanium Processor, Concluding Remarks.

Unit 4:Large-Scale Multiprocessors and Scientific Applications Introduction, Interprocessor Communication [16]

The Critical Performance Issue, Characteristics of Scientific Applications, Synchronization: Scaling Up, Performance of Scientific Applications on Shared-Memory

Multiprocessors, Performance Measurement of Parallel Processors with Scientific Applications,

Implementing Cache Coherence, the Custom Cluster Approach: Blue Gene/L, Concluding Remarks.
Computer Arithmetic: Introduction, Basic Techniques of Integer Arithmetic, Floating Point, Floating-Point Multiplication, Floating-Point Addition, Division and Remainder, More on Floating-Point Arithmetic, Speeding Up Integer Addition, Speeding Up Integer Multiplication and Division, Fallacies and Pitfalls.

References:

1. Hennessey and Patterson, "**Computer Architecture A Quantitative Approach**", 4th Edition, Elsevier, 2007.
2. Kai Hwang, "**Advanced Computer Architecture - Parallelism, Scalability, Programmability**", 2nd Edition, 1992.

Semester – III

Course Code	Course Title	Duration		L	T	P	C
MTVS15F3110	MSP430	14 Weeks	SC	4	0	1	5

Prerequisites:

1. Knowledge on basics of MSP430 architecture.
2. Concepts of Interrupts and Interfacing techniques in MSP430.
3. Basic knowledge of I^2C and serial communication.
4. Practical knowledge on MSP430 programming.

Course Objectives:

1. Study the introduction to the TI MSP430 family of microcontrollers, their architecture, peripheral features and programming.
2. Understand and Provide theoretical and practical aspects of low-power system development using the MSP430.
3. Know the peripheral features of the MSP430, which include timers, digital and analog IO and serial communication modules.
4. Understand and Present case studies of application of the MSP430 so that the student can handle embedded system design projects independently.
5. Know the applications of the MSP430 in embedded systems.

Course Outcomes:

On completion of this course the students will be able to:

1. Design, develop, and evaluate software or a software/hardware system, component, or process to meet desired needs within realistic constraints.
2. Demonstrate and function on multi-disciplinary teams working in mechatronics and low power embedded systems.
3. Design, identify, formulate, and solve engineering problems
4. Analyse the need for, and an ability to engage in life-long learning and continuing professional development
5. Analyse a problem, and identify and define the computing requirements appropriate to its solution.
6. Design and develop principles in the construction of software systems of varying complexity.

Mapping of Course Outcomes with Program Outcomes

Course Code	POS/ COs	PO1	P 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
MTVS15F 3110	CO1	3	1	1	1			3					3	3	2	2
	CO2	2	1	2	1			3					3	3	2	1
	CO3	2	1	2				3					3	3	2	2
	CO4			3				3					3			2
	CO5	2	1	2				3					3	3	2	2
	CO6	2	1	2				3					3	3	2	2

Course Contents:

Unit 1:MSP430 Architecture and Programming [16]

Architecture of the MSP430, addressing modes, instruction set, development environment, MSP430 programming in C and assembly language.

Unit 2:Interrupts and Digital IO in the MSP430 [16]

Interrupts, interrupt service routines, low-power modes of operation, parallel ports, digital inputs, and outputs, driving heavier loads, liquid crystal displays, driving an LCD from an MSP430x4xx.

Unit 3: Timers and Analog IO in the MSP430 [16]

Watchdog timer, basic timer1, timer_A, measurement in the capture mode, pulse-width modulation, modes of timer_A and timer_B, comparator_A, basic operation of the ADC10 and ADC12, the SD16_a sigma–delta ADC.

Unit 4:Communication Peripherals the MSP430 [16]

SPI and I^2C features in MSP430, asynchronous serial communication, case studies of the applications of the MSP430 in embedded systems.

References:

1. John Davies, "**MSP430 Microcontroller Basics**", Newnes (Elsevier Science), 2008.
2. C P Ravikumar, "**MSP430 Microcontroller in Embedded System Project**," Elite Publishing House Pvt. Ltd., December 2011.
3. **MSP430 Teaching CD-ROM**, Texas Instruments, 2008.
4. Sample Programs for MSP430 downloadable from *www.msp430.com.*

Course Code	Course Title	Duration		L	T	P	C
MTVS15F3120	FPGA Based Embedded System	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Concepts of digital system design and behaviour modelling of a system.
2. Basics of Verilog and VHDL.
3. FPGA architecture and its technologies.
4. Knowledge of sequential and combinational circuits.

Course Objectives:

1. Understand Digital system design using HDL.
2. Know FPGA architecture, interconnect and technologies.
3. Know different FPGA's and implementation methodologies.
4. Understand configuring and implementing digital embedded system, microcontrollers, microprocessors, DSP algorithm on FPGA.

Course Outcomes

On completion of the course the students will be able to:

1. Design reconfigurable digital systems.
2. Demonstrate and Debug the embedded systems before the actual product is developed.
3. Design finite state machines for various applications.
4. Design dynamic architectures using FPGA's
5. Implement, Design and develop embedded system using EDA tools.

Mapping of Course Outcomes with Programme Outcomes

Course Code	POS / COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
	CO1	3	3	3		2				2	3		3	2	3	2
	CO2	3	3	3		2				2	3		3	2	3	2
	CO3	3	3	3		2				2	3		3	2	3	2
	CO4	3	3	3		2				2	3		3	2	3	2
	CO5	3	3	3		2				2	3		3	2	3	2

Course Contents:

Unit 1: Introduction [16]

Digital system design options and tradeoffs, Design methodology and technology overview, High Level System Architecture and Specification: Behavioral modelling and simulation, Hardware description languages, combinational and sequential design, state machine design, synthesis issues, test benches.

Unit 2:Overview of FPGA architectures and technologies [16]

FPGA Architectural options, granularity of function and wiring resources, coarse vs fine grained, vendor specific issues (emphasis on Xilinx and Altera), Logic block architecture: FPGA logic cells, timing models, power dissipation I/O block architecture: Input and Output cell characteristics, clock input, Timing, Power dissipation.

Unit 3: Placement and Routing [16]

Programmable interconnect - Partitioning and Placement, Routing resources, delays; Applications - Embedded system design using FPGAs, DSP using FPGAs, Dynamic architecture using FPGAs, reconfigurable systems, application case studies.

Unit 4: Applications [16]

Simulation/implementation exercises of combinational, sequential and DSP kernels on Xilinx/Altera boards.

References:

1. M.J.S. Smith, "**Application Specific Integrated Circuits**", Pearson, 2000.
2. Peter Ashenden, "**Digital Design using VHDL**", Elsevier, 2007.

3. Peter Ashenden, "**Digital Design using Verilog**", Elsevier, 2007.
4. W.Wolf, "**FPGA based system design**", Pearson, 2004.
5. Clive Maxfield, "**The Design Warriors's Guide to FPGAs**", Elsevier, 2004.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F3130	Advanced Digital Systems Design	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Basics of microelectronics, semiconductor technologies.
2. Concepts of system modelling and different optimizations of combinational logic circuit.
3. Knowledge on transformations, synthesis and delay calculation for combinational circuit.
4. Basics of scheduling algorithm.

Course Objectives:

1. To understand different methods used for the simplification of Boolean functions.
2. To understand and implement combinational, synchronous, and asynchronous sequential circuits.
3. To be acquainted with the MOS devices, system level design.
4. To outline the formal procedures for the analysis and design of combinational circuits and sequential circuits using computer aided synthesis.
5. To provide hands on experience to the concepts taught in class.

Course Outcomes:

On completion of this course the students will be able to:

1. Design combinational and sequential circuits.
2. Differentiate between Mealy and Moore model state machines, and draw a block diagram of each.
3. Describe the operation of basic logic gates (NOT, NAND, NOR) constructed using N- and P-channel MOSFETs and draw their circuit diagrams.
4. Define logic gate fan-in and describe the basis for its practical limit.
5. Calculate the DC noise immunity margin of a logic circuit and describe the consequence of an insufficient margin.
6. Design and demonstrate some basic projects based on sequential design.

Mapping of Course Outcomes with Programme Outcomes

Course Code	POS / COs	PO 1	PO2	PO3	PO4	PO5	PO 6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
MTVS15F3130	CO1	3	3	3		2				2	3		3	2	3	2
	CO2	3	3	3		2				2	3		3	2	3	2
	CO3	3	3	3		2				2	3		3	2	3	2
	CO4	3	3	3		2				2	3		3	2	3	2
	CO5	3	3	3		2				2	3		3	2	3	2
	CO6	3	3	3		2				2	3		3	2	3	2

Course Contents

Unit 1:Introduction **[16]**

Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization.

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

Unit 2:Hardware Modeling **[16]**

Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.

Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.

Unit 3:Multiple Level Combinational Optimizations **[16]**

Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.

Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Unit 4:Schedule Algorithms **[16]**

A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

Cell Library Binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding.

References:

1. Giovanni De Micheli, "**Synthesis and Optimization of Digital Circuits**", Tata McGraw-Hill, 2003.
2. ZviKohavi, "**Switching and Finite Automata Theory**", Tata McGraw Hill, thirdedition, 2000.
3. Alan B.Marcovitz, "**Intro. To Logic Design**", TMH, second edition, 2002.
4. Srinivas Devadas, Abhijit Ghosh, and Kurt Keutzer, "**Logic Synthesis**", McGraw-Hill, USA, 1994.
5. Neil H.E. Weste and David money harris, "C**MOS VLSI Design: A circuits and system Perspective**",fourth edition, Pearson Education (Asia) Pvt. Ltd., 2000.
6. Kevin Skahill, "**VHDL for Programmable Logic**", Pearson Education (Asia) Pvt. Ltd., 2000.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F3140	CMOS RF Circuit Design	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Concepts of RF design and wireless technology.
2. Basic knowledge on RF modulation techniques.
3. Knowledge on behaviour and characteristics of BJT and MOSFET.

Course Objectives:

1. Understanding of the design and analysis of radio frequency integrated circuits and systems (RFICs) for communication.
2. Integrated Electronic Circuit Design which covers transistor-level design.

Course Outcomes:

On completion of this course the student will be able to:

1. Describe and understand the general challenges in the design of CMOS RF circuits.
2. Design matching circuits using passive RLC components.
3. Use various techniques to design high-frequency amplifiers.
4. Design and analyze oscillators.
5. Understand fundamentals of phase noise in oscillators.

Course Code	POs/ COs	PO1	PO2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
MTVS15F3140	CO1	3	3	3	3								2	3	3
	CO2	3	2	2	3								2	3	3
	CO3	4	2	3	2	4							2	3	3
	CO4	3	3	3	3	2		2					3	3	3
	CO5	3	3	3	3	2		2					3	3	3

Course Contents:

Unit 1: Introduction to RF Design and Wireless Technology **[16]**

Design and Applications, Complexity and Choice of Technology.

Basic concepts in RF design: Nonlinearly and Time Variance, Inter symbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion.

Unit 2: RF Modulation **[16]**

Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, direct conversion and two-step transmitters.

Unit 3: BJT and MOSFET Behavior at RF Frequencies **[16]**

BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation.

Unit 4: RF Circuits Design **[16]**

Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures

And frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

References:

1. B. Razavi, "**RF Microelectronics**" PHI 1998.
2. R. Jacob Baker, H.W. Li, D.E. Boyce "**CMOS Circuit Design, layout and Simulation**", PHI 1998.
3. Thomas H. Lee "**Design of CMOS RF Integrated Circuits**" Cambridge University press 1998.
4. Y.P. Tsividis, "**Mixed Analog and Digital Devices and Technology**", TMH 1996.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F3150	Advances in VLSI Design	16 Weeks	SC	4	1	0	5

Prerequisites:

1. Concepts of MOS and CMOS circuits.
2. Knowledge on BICMOS, steering logic and buffers.
3. Differences between MOS and CMOS.
4. Concepts of various design methods in CMOS.

Course Objectives:

1. To understand the basics and operation of static, comparison between CMOS and

BiCMOS.

2. To understand short channel effects.
3. To understand the challenges to CMOS.
4. To understand the super buffers, layouts and technology mapping.

Course Outcomes

On completion of this course the student will be able to:

1. Learn advanced technologies in the fields of VLSI design with the fundamental concepts.
2. Apply advanced technical knowledge in multiple contexts.
3. Understand and design advanced VLSI based system and analyse and interpret results.
4. Use the techniques, skills, modern Electronic Design

Mapping of Course Outcomes with programme Outcomes

Course Code	POS / COs	PO 1	P0 2	PO 3	PO 4	PO 5	PO 6	P 7	PO 8	P O 9	P O 1 0	P O 1 1	P O 1 2	PS O 1	PSO 2	PSO 3
MTVS15 F3150	**CO1**	**1**		**2**			**3**							**3**	**1**	**2**
	CO2		**1**	**2**			**3**							**2**	**1**	**3**
	CO3				**2**	**1**	**3**							**3**	**2**	**1**
	CO4		**2**	**1**	**3**											

Course Contents:

Unit 1: Review of MOS Circuits **[16]**

MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS.

Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS Miniaturization.

Unit 2: Beyond CMOS **[16]**

Evolutionary advances beyond CMOS, carbon Nanotubes, conventional vs. tactile computing, computing, molecular and biological computing - molecular Diode and diode- diode logic. Defect tolerant computing.

Super Buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks -NMOS and CMOS functional blocks.

Unit 3: Special Circuit Layouts and Technology Mapping **[16]**

Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module layout.

Unit 4:System Design **[16]**

CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable

inter connect, programmable structure, Gate arrays standard cell approach, Full custom design.

References:

1. Kevin F Brennan "**Introduction to Semi-Conductor Device**", Cambridge publications, 2006.
2. Eugene D Fabricius "**Introduction to VLSI Design**", McGraw-Hill International publications, 1990.
3. D.APucknell. "**Basic VLSI Design**", PHI Publication, 2005.
4. Wayne Wolf, "**Modern VLSI Design**" Pearson Education, Second Edition, 2002.

Course Code	Course Title	Duration		L	T	P	C
MTVS15F3400	AUTOMOTIVE ELECTRONICS SYSTEM	16 Weeks	OE	3	1	0	4

Course Objectives:

1. Understand the functions of electronic systems in modern automobiles, modern electronics technology to improve the performance, safety, comfort and related issues
2. Study the principles of automotive sensors and interfacing techniques, design, model and simulate interfacing systems with sensors
3. Know the principles and functionalities of various Automotive Communication Protocols (ACPs), Design ACP based In-Vehicle Networks(IVNs), selection of ACPs for various application in Automotive
4. Know the industry standard practices for ECU design for automotive, modeling and analysis of application software for ECU design and development, design of ECUs for automobiles, design of HIL and fault diagnostics

Course Outcomes:

1. Implement and Interface sensors and for various automotive applications
2. Design and diagnose the faults in the systems Implement automotive fault diagnostics and faults
3. Analyze on and off board diagnostics, diagnostics protocol.

Mapping of Course Outcomes with Program Outcomes

4.

Course Code	POs/ COs	PO1	PO 2	PO3	PO4	PO5	PO6	P7	PO8	PO9	PO 10	PO 11	PSO 1	PSO 2	PSO 3
MTVS15F3 400	CO1	2	1					2				3	1		2
	CO2	1	2	1		3			3				1		2
	CO3	1		1			2				3		1		2

Course Contents:

UNIT 1:Automotive Industry and Modern Automotive Systems [12]

Vehicle classifications and specifications, need for electronics in automobiles, Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Spark and Compression Ignition Engines, Ignition systems, Spark plug, Spark pulse generation, Ignition Timing. Transmission

Control - Automotive transmissions, Drive Train, Brakes, Steering System - Steering Control, Starting System- Battery, Air/Fuel Systems, Fuel Handling, Air Intake System, Lighting.

UNIT 2:Introduction to Automotive Sensors and Instrumentation [12]

Sensors and actuators, Air/ Fuel Management Sensors – Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor - Strain gauge and Capacitor capsule, Engine Coolant Temperature (ECT) Sensor, Intake Air Temperature (IAT) Sensor, Knock Sensor, Airflow rate sensor, Throttle angle sensor Sensors in Engine control, adaptive cruise control, braking control, traction control, steering, stability, Lighting, wipers, climate control, Sensors for occupant safety, Sensor and actuator interfacing techniques and electronic displays. Actuators – Fuel Metering Actuator, Fuel Injector, Ignition Actuator

UNIT 3:Control Systems [12]

Exhaust After-Treatment Systems – AIR, Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle sped control, EGR Control Communication – Serial Data, Communication Systems, Power windows, Remote keyless entry systems, GPS,Automotive Communication Protocols Protection, Body and Chassis Electrical Systems, Remote Keyless Entry, Vehicle Motion Control – Cruise Control, Chassis, , Power Brakes, antilock braking systems, Electronic stability and other technologies, Traction Control, Electronic Stability Control, Electronically controlled suspension Fundamentals of electronically controlled steering system, Power Steering,

UNIT 4: Safety and Convenience [12]

Electronics for Passenger Safety and Convenience – SIR, Air bag and seat belt pretension systems, Tire pressure monitoring systems, Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters Integrated Body – Climate Control Systems, Electronic HVAC Systems, Lighting, Entertainment Systems Automotive Diagnostics – Timing Light, Engine Analyzer, Process of Automotive Fault Diagnostics, Fault Codes, On-board diagnostics, Off-board diagnostics, Expert Systems. Future Automotive Electronic Systems – Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System, AFS.

Reference Books:

1. Denton.Burlington "**Automotive Electrical and Electronic Systems**", MA 01803, Elsevier Butterworth-Heinemann, 2004.
2. Ronald K. Jurgen. "**Automotive Electronics Handbook**", 2nd Edition, McGraw-Hill, 2007
3. Christian Kohler, "**Enhancing Embedded Systems Simulation**" Vieweg+TeubnerVerlag/ Springer, 2011.
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SCHOOL WISE INFORMATION ABOUT THE FACULTY IN THE FORMAT PROVIDED BY THE UGC

Name of Department : School of Electronics and Communication Engineering (UG)

Sl.No.	Name of Teacher	Designation	Qualification	Experience	Date of Joining
1	Dr. R. C. Biradar	Professor	ME, Ph. D	26	31.10.2007
2	Dr.Bharathi S H	Professor	M.Tech, Ph D	24	7.2.2012
3	Dr.Geeta. D	Professor	M.Tech, Ph D	20	31.10.2007
4	Dr.MrinalSarvagya	Professor	ME, Ph. D	18	16.10.2014
5	Dr.VishuKumar.M.	Professor	M.Sc, Ph. D	16	23.08.2008
6	Dr.P. I. Basarkod	Professor	ME, (Ph. D)	29	12.02.2009
7	Seetha Rama Raju S	Associate Professor	M.Tech (Ph. D)	30	11.07.2011
8	Nayana D. K	Associate Professor	M.Tech (Ph. D)	19	24.08.2009
9	Bharathi Devi	Associate Professor	M.Sc, M. Phil	23	14.06.2004
10	Dr.Dilip Kumar Sar	Associate Professor	M Sc, M. Phil, Ph. D	17	01.06.2004
11	Dr.Madesh Kumar	Associate Professor	M.Sc, M. Phil, Ph. D.	16	13.08.2013
12	Dr.Vasantha D M	Assistant Professor	M Sc, Ph. D	8	01.08.2012
13	Dr.Srikumar	Assistant Professor	M Sc, Ph. D	11	29.07.2013
14	Dr.Naresh Kumar	Assistant Professor	M Sc, Ph. D	3	01.07.2015
15	Manjunath R Kounte	Assistant Professor	M.Tech, (Ph. D)	8	08.10.2010
16	Mohammed Riyaz Ahmed	Assistant Professor	M.Tech, PGDBA, (PhD)	8	01.04.2011
17	ShrikantTangade	Assistant Professor	M.Tech , (Ph. D)	6	31.12.2011
18	Divya M. N	Assistant Professor	M.Tech , (Ph. D)	13	01.08.2011
19	Neethu K N	Assistant Professor	M.Tech	4	30.07.2012
20	Pratibha V Hegde	Assistant Professor	M Tech	8	16.06.2014

21	WarshaBalani	Assistant Professor	M Tech	6	12.06.2014
22	Sarveda S	Assistant Professor	M Tech	3	12.09.2014
23	Abdul Haq N	Assistant Professor	M Tech (CS)	3	15.09.2014
24	Jyothy S T	Assistant Professor	M Tech	6	15.09.2014
25	K Vishnu Vardhan Reddy	Assistant Professor	M Tech	3	15.06.2015
26	Ashwini P	Assistant Professor	M Tech	2	15.06.2015
27	Tanweer	Assistant Professor	M Tech	1	15.06.2015
28	Susan Thomas	Assistant Professor	M Tech	2	15.06.2015
29	Raghu K	Assistant Professor	M Tech	3	15.06.2015
30	SowmiyaBharani B	Assistant Professor	ME	2	15.06.2015
31	Ravi Shankar D	Assistant Professor	M Tech	4	15.06.2015
32	Gloria Nandihal	Assistant Professor	M Tech	4	01.07.2015
33	Bharath H P	Assistant Professor	M Tech	1	24.07.2015
34	Anupama R	Assistant Professor	M Tech	1	27.07.2015
35	SugandhaSaxena	Assistant Professor	M Tech	3	01.08.2015
36	Anil Kumar V	Assistant Professor	M Tech	1	16.09.2015
37	Madan .H.T	Assistant Professor	M Tech	6	01.07.2016
38	Debarti Bhattacharya	Assistant Professor	M.Tech , (Ph. D)	9.5	01.07.2016
39	Praveen	Teaching Associate	M. Tech.	0	01.07.2016
40	Sunil M. D.	Teaching Associate	M. Tech.	0	01.07.2016
41	Uday Kumar	Assistant Professor	M Sc, M. Phil	17	13.07.2007
42	A Mubeena	Assistant Professor	M Sc.	4	27.07.2015
43	Ragini.B.S	Assistant Professor	M Sc., Phil	6	27.07.2015
44	Varalakshmi.G	Assistant Professor	MA	1	28.01.2015
45	Meera Nair	Assistant Professor	MA, PGCTE, PGDTE	6	18.03.2015

Name of Department : School of Electronics and Communication Engineering (PG)

Sl.No.	Name of Teacher	Designation	Qualification	Experience	Date of Joining
1	Dr. R Venkata Siva Reddy	Professor	M.Tech, PhD	24	27.06.2012
2	Dr. G Seshikala	Professor	ME, Ph D	23	01.08.2015
3	Dr.Veena.K.N	Assiociate Professor	M.Tech. PhD	16	18.04.2016
4	P R Savitha	Assiociate Professor	ME, (Ph D)	21	03.08.2007
5	S N Prasad	Associate Professor	M.Tech(PhD)	20	02.07.2012
6	Sudarshan K. M	Associate Professor	M.Tech (Ph.D)	14	15.02.2007
7	L Nirmala	Assistant Professor	M.Tech (Ph.D)	11	21.01.2009
8	Prashanth V Joshi	Assistant Professor	M.Tech (Ph.D)	6	03.08.2009
9	MdTauseef	Assistant Professor	M Tech	1	14.09.2015

DO'S AND DON'TS

DO'S

- Maintain discipline and respect the rules and regulations of the university
- Be regular and punctual to classes
- Study regularly and submit assignments on time
- Be respectful to your colleagues/friends and hostel staff/management.
- Read the notice board (both at your college and the hostel) regularly.
- Utilize your Personal Computer for educational purpose only.
- Follow the code of conduct.
- Visit Health Center on the campus whenever you are unwell.
- Be security conscious and take care of your valuables especially Cash, Mobile Phones,
- Laptop and other valuables.
- Carry your valuables along with you whenever you proceed on leave/vacation.
- Use electric appliances, lights and water optimally.
- Keep the campus clean and hygienic.

DON'TS

- Ragging inside / outside the campus.
- Possession of Fire arms and daggers etc.
- Use of Alcohols, Toxic drugs, sheesha, gutkha and hashish/heroin etc.
- Use of Crackers, explosives and ammunition etc.
- Smoking and keeping any kind of such items.
- Misusing college & hostel premises/facilities for activities other than studies.
- Playing loud music in the room which may disturb studies of colleagues / neighbours.

- Making noise and raising slogans.
- Keeping electrical appliances, other than authorized ones.
- Involvement in politics, ethnic, sectarian and other undesirable activities.
- Proxy in any manner.
- Use of mobiles in the classrooms.

Note: 1. Rules are revised / reviewed as and when required.

2. Healthy suggestions are welcome for betterment of Institution