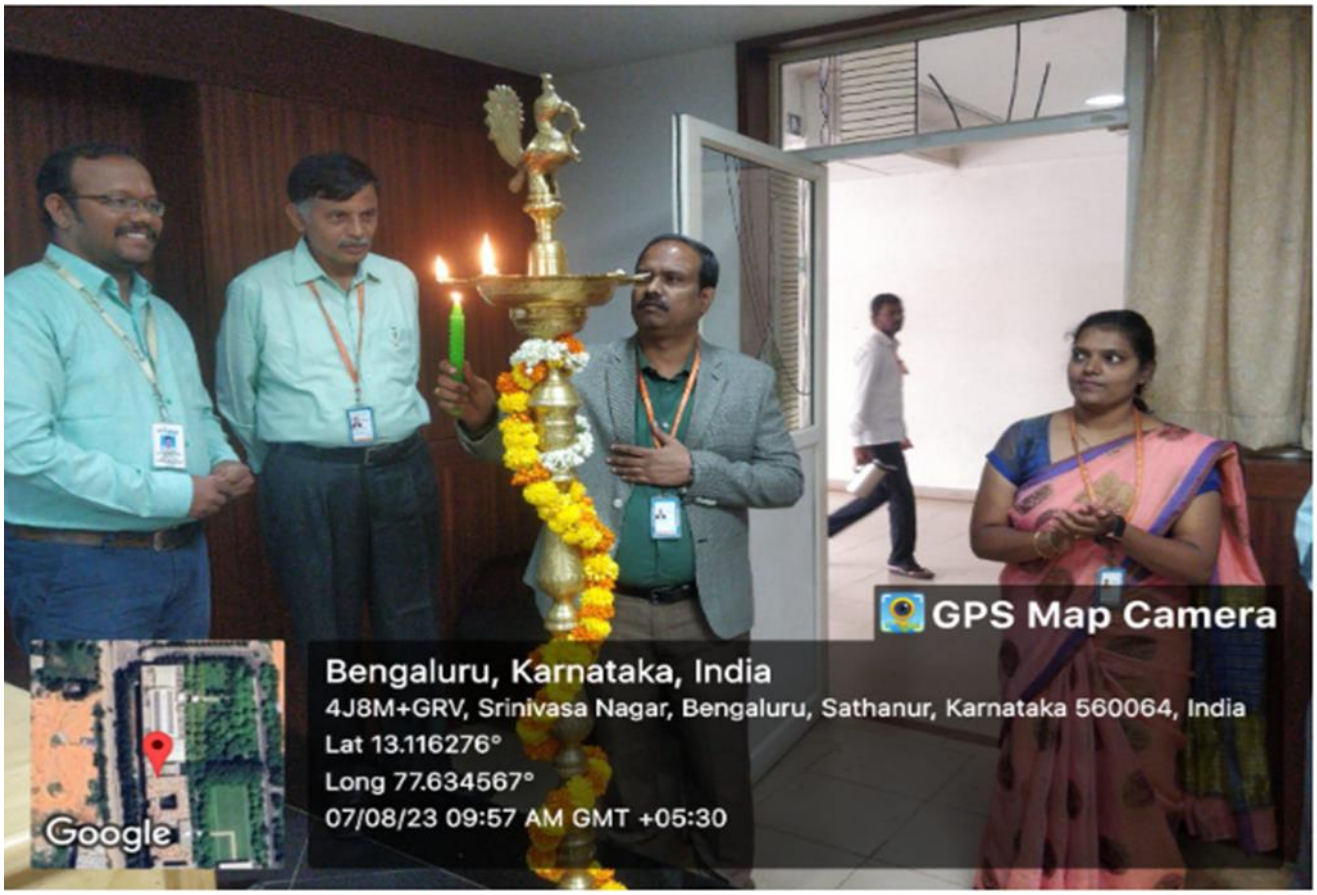
REVA UNIVERSITY
Bengaluru, India
Established as per the section 2(f) of the UGC Act, 1956,
Approved by AICTE, New Delhi

SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

Organized a "Five Day FDP
On
"Hands - on Analog and Digital IC Design using Cadence Tools"

Date	**7th August 2023 to 11th August 2023**
Title	**"Hands - on Analog and Digital IC Design using Cadence Tools"**
School	Electronics and Communication Engineering
Resource Person	Mr. Shivaprasad B K, Sr. FAE, Entuple Technologies Pvt. Ltd, Bengaluru • Dr. Mamidi Nagaraja, Technical Manager, Entuple Technologies Pvt. Ltd, Bengaluru • Dr. K M Sudarshan, Professor, REVA University, Bengaluru. • Dr.Prashanth Joshi, Associate Professor, REVA University, Bengaluru • Dr.Prameela Kumari, Associate Professor, REVA University, Bengaluru • Dr. Shashank Dwivedi, Associate Professor, REVA University, Bengaluru • Dr.A. Raganna, Associate Professor, REVA University, Bengaluru • Prof.RaJi C, Assistant Professor, REVA University, Bengaluru
Venue	Aryabhatta Seminar Hall, CV RAMAN Block, REVA University
Targeted Audience	**PG Students** Research Scholars, Faculty of engineering colleges
No. of Participants	35
About the event	**School of ECE** organized a Five Day FDP On "Hands - on Analog and Digital IC Design using Cadence Tools" 7th August 2023 to 11th August 2023 This workshop will give exposure to Analog and Digital VLSI Design Logic to Layout, aim to introduce the most demand skills in VLSI. This FDP deals with the fundamental theory to Practical hand on training in VLSI and it is lead by industry experts, which would provide Participants to learn from the scratch to write code, design using the CMOS transistors which help them to manage their projects efficiently and make the career as a VLSI design engineer.
Description	The following technical and hands on topics are covered by our experts • Introduction to Full Custom and Semi-Custom IC Design Flow • Cadence Solutions for Full Custom and Semicustom IC Design • Test bench Creation using Virtuoso Schematic Editor • Functional Simulation using Spectre

	• Layout Design using Virtuoso Layout Editor • Physical Verification which includes DRC & LVS • Post Layout Simulation • RTL Synthesis using Genus Synthesis Solution • Physical Implementation using Innovus that includes • Floor Planning ✓ Power Planning ✓ Placement ✓ CTS ✓ Routing • Timing Analysis • Power Analysis • Parasitic Extraction • Generation of GDSII
Out Come of the Session	**The primary objectives of this FDP are** ➢ To acquire knowledge and skill sets in the field of latest VLSI Technology ➢ To improve your Technical competency by using Industry standard VLSI tools and hardware ➢ To stay relevant and disseminate the acquired knowledge to your student community ➢ To enhance career growth in core domain Give exposure to current trends and research challenges **Event Outcomes (Course Outcome):** ➢ Understand the fundamentals in the field of EDA Tools. ➢ Understand new areas of research and development which is VLSI tools and hardware ➢ Acquire the research competence in the areas like VLSI Technology
FeedBack Analysis	PG Students and Faculties have expressed their overwhelming feedback response with a rating as a good. They have felt that the hands on session was very educative and informative. They have also expressed their concent for attending many more such FDPs on this domain in future.
Coordinators	Dr. Venkateshappa, Professor, School of ECE. Dr.Seshikala, Professor, School of ECE
Director	Dr. K.M. Sudarshan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