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Dr. P. Shyama Raju
Chancellor, REVA University

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Patrons

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Vice Chancellor, (I/C)

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Dr. Rajashekar C. Biradar
Pro Vice Chancellor
(Engineering), REVA University

Dr. Narayana Swamy
Registrar, (I/C)

Convener

Dr. Ashwin Kumar U. M.
Director, School of CSE

Coordinators

Dr. Sanju V.
Professor, School of CSE, REVA University

Dr. Prabhuraj
Assistant Professor, School of CSE, REVA University

Advisory Commitee

Mr.Padmanabhan, Intel Technology, India
Dr. Basavaraj Talwar, NITK
Dr. Goutam Sanyal REVA University
Dr. Arun Biradar, REVA University

Committee Members

- Dr. Bhaskar Reddy, School of CSE
- Dr. Argha Sarkar, School of CSE
- Dr. Mayuri, School of CSE
- Prof. Thirumagal E, School of CSE
- Prof. Madhumitha, School of CSE
- Dr. Amuthabala, School of CSE
- Dr Naveen Chandra Gowda, School of CSE
- Dr. Supreeth S, School of CSE
- Prof. Nithin Ramakrishnan, School of CSE
- Prof. Narendra Babu, School of CSE
- Dr. Neelam Malyadri, School of CSE
- Dr. Anooja Ali, School of CSE

Important Dates

The workshop is scheduled to be organised from
26th August, 2024 to
31st August, 2024

Registration Details

Registration Fee

No registration fee for this course

Contact

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Asst. Prof, School Of CSE, REVA University.
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REVA UNIVERSITY

Bengaluru, India

AICTE Training and Learning (ATAL)Academy Sponsored Six-day Faculty Development Program on

Digital Design Using Intel FPGA

26th to 31st August, 2024

Organised by
School of Computer Science & Engineering

Rukmini Knowledge Park,
Kattigenahalli, Yelahanka, Bengaluru-560064
Phone:+91-80-4696 6966

Rukmini Educational
Charitable Trust

www.reva.edu.in

About REVA University

REVA University is a State Private University established in Karnataka State under the Government of Karnataka Act No. 13 in the year 2012 in Bengaluru, the IT capital of India. REVA University, recognised by the University Grants Commission (UGC) and approved by the All India Council for Technical Education (AICTE), has an A+ grade from NAAC.

REVA University prides itself in contributing to every student's holistic development. The University currently offers 38 full-time undergraduate programmes, 33 full-time postgraduate programmes, 20 PhD programmes, and certification and diploma programmes. The University offers programmes in Engineering, Architecture, Science and Technology, Commerce, Management Studies, Law, Arts & Humanities, and Performing Arts. Courses are offered in Certificate/Diploma and Post Graduate Diploma too. REVA University facilitates research leading to a Doctoral Degree in all disciplines. The programmes offered by REVA University are well-planned and designed based on methodical analysis and research with emphasis on knowledge assimilation, practical applications, hands-on training, global and industrial relevance, and their social significance.

Teachers and instructors with illustrious academic experience are the architects of the meticulously designed curriculum and program modules offered at REVA University. They come with industrial exposure and experience that often translates through their teaching, thus bridging the gap between the industry and academia.

About the School

The School of Computer Science and Engineering, headed by an eminent professor supported by well qualified and expe- rienced faculty members. The school has the state-of-the-art classrooms and advanced computer laboratories. The school offers M. Tech in Computer Science & Engineering (Full Time),

M. Tech in Computer Science & Engineering (Part Time), and B. Tech in Computer Science & Engineering and B. Tech in AI and Data Science. The curriculum of both graduate and post graduate degree programs have been designed to bridge the gap between industry – academia and hence they are industry oriented. These programs provide ample scope to enter a wide range of business opportunities. This is reflected in various core subjects offered within the program.

Vision

School of Computer Science and Engineering aspires to become an innovative technological hub by developing excel- lent human resources in computer science and engineering through education of global standards that instills technical competence, leadership qualities, ethical and moral values, research and innovation skills, societal commitment, and entrepreneurship abilities.

About The Workshop

FPGA programming entails designing digital circuits on Field-Programmable Gate Arrays. It involves defining logic functions and interconnections within the FPGA's configu- rable hardware. Programmers utilize Hardware Description Languages like Verilog or VHDL to specify the desired behav- ior. FPGAs offer flexibility and reconfigurability, making them suitable for diverse applications. Efficient FPGA programming demands optimization for performance, power consumption, and resource utilization.

Intel FPGAs boast industry-leading performance and power efficiency. They are renowned for their versatility, catering to a wide range of applications from data centers to IoT devices. In this workshop we will be introducing the Intel Quartus tool with the different support utilities to make programming on FPGA simpler.

Objectives of FDP

FPGA programming entails designing digital circuits on Field-Programmable Gate Arrays. It involves defining logic functions and interconnections within the FPGA's configu- rable hardware. Programmers utilize Hardware Description Languages like Verilog or VHDL to specify the desired behav- ior. FPGAs offer flexibility and reconfigurability, making them suitable for diverse applications. Efficient FPGA programming demands optimization for performance, power consumption, and resource utilization.

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Topics Covered

- Introduction To ASIC World
- Introduction To FPGA
- Programming FPGA
- Introduction to Intel Quartus
- Different tools used with intel Quartus
- Introduction to NIOS processor
- Research In the area of FPGA

Resource Persons

- Mr. Padmanabhan, Intel Technologies, Bangalore
- Dr. Basavaraj Talvar, NITK
- Dr. Sanju V, REVA University, Bangalore
- Dr. Nitish Kumar, VIT Vellore

Registration Form

The number of participants will be limited to 50 only.

Registration Fees: Free

Mode of Delivery: Offline

Participants can sign up and register for the program in AICTE-ATALwebsite. Website Links:

https://www.aicte-india.org/atal OR

https://atalacademy.aicte-india.org/signup

A test shall be conducted by coordinator at the end of the program. The certificate shall be issued to those participants who have attended the program with 100% attendance and scored minimum 80% marks in the tes

Schedule of BASIC FDP

FDP Application Number : 1715055083
Title of the FDP: Digital Design Using Intel FPGA
FDP Start Date : August 26th 2024
FDP End Date: August 31st 2024

Day 1	Day 2	Day 3	Day 4	Day 5	Day 6
9:00 AM – 9:30 AM **Inauguration**					
9:30 AM – 12:00 Noon **Session 1** 1. **Name of the Expert :** Dr. Sudharshan 2. **Designation :** *Professor* 3. **Organization:** *REVA University* 4. **Experience in Years:** 22 5. **Topic to be taught:** *Fundamentals Of FPGA*	**9:30 AM – 12:00 Noon** **Session 3** 1. **Name of the Expert :** Padmanaban K 2. **Designation : Enabling & Optimization Engineer** 3. **Organization:** *Intel Technology India Private Limited* 4. **Experience in Years: 18** 5. **Topic to be taught:** *Introduction to Simulations for FPGA*	**9:30 AM – 12:00 Noon** **Session 5** 1. **Name of the Expert :** *Intel Technology India Private Limited* 2. **Designation** : *IP Engineer* 3. **Organization:** *Intel Technology India Private Limited* 4. **Experience in Years:** *18* 5. **Topic to be taught:** *Introduction to SOC*	**9:30 AM – 12:00 Noon** **Session 7** 1. **Name of the Expert :** *Intel Technology India Private Limited* 2. **Designation** *: IP Engineer* 3. **Organization:***Intel Technology India Private Limited* 4. **Experience in Years:** *18* 5. **Topic to be taught:** *Artificial Intelligence on FPGA*	**9:30 AM – 12:00 Noon** **Industrial visit** 1. **Name of the Organization:** *Intel Technology India Private Limited* 2. **Complete address with pincode :** *#136, HAL Old Airport Road, Kodihalli, Bengaluru – 560017* 3. **Industry Type:** *VLSI* 4. **Area of specification :** *Processor/ Reprogrammable Devices*	**9:30 AM – 12:00 Noon** **Session 10** 1. **Name of the Expert :** Basavaraj Talwar. 2. **Designation : Assistant Professor** 3. **Organization: NITK, Surathkal** 4. **Experience in Years:** 20 5. **Topic to be taught:** *Academic Research in FPGA*
12:00 Noon – 1:00 PM **Article Discussion** **1.Title of the Research Paper :** *Design and Implementation of FPGA-Based Systems - A Review* **2. Name of the journal:** *Australian Journal of Basic and Applied Sciences* **3. Year of Publication:** *2009*	**12:00 Noon – 1:00 PM** **Article Discussion** **1.Title of the Research Paper :** *A Simple Processor* **2. Name of the journal:** *Intel FPGA Academy* **3. Year of Publication:** *2020*	**12:00 Noon – 1:00 PM** **Article Discussion** **1.Title of the Research Paper :** *Introduction to Graphics and Animation* **2. Name of the journal:** *Intel FPGA Academy* **3. Year of Publication:** *2020*	**12:00 Noon – 1:00 PM** **Article Discussion** **1.Title of the Research** *Paper :FPG-AI: A Technology-Independent Framework for the Automation of CNN Deployment on FPGAs* **2. Name of the journal:** *IEEE Access* **3. Year of Publication:** ***2023***		**12:00 Noon – 1:00 PM** **Article Summary**
1:00 PM – 2:00 PM **Lunch**	**1:00 PM – 2:00 PM** **Lunch**	**1:00 PM – 2:00 PM** **Lunch**	**1:00 PM – 2:00 PM** **Lunch**	**1:00 PM – 2:00 PM** **Lunch**	**1:00 PM – 2:00 PM** **Lunch**
2:00 PM – 4:30 PM **Session 2** 1. **Name of the Expert :** *Padmanaban K* 2. **Designation** *: Software Enabling & Optimization Engineer* 3. **Organization:** *Intel Technology India Private Limited* 4. **Experience in Years:** *18* 5. **Topic to be taught:** *Introduction to Intel Quartus*	**2:00 PM – 4:30 PM** **Session 4** 1. **Name of the Expert :** *Padmanaban K* 2. **Designation :** *Enabling & Optimization Engineer* 3. **Organization:** *Intel Technology India Private Limited* 4. **Experience in Years***: 18* 5. **Topic to be taught:** *Working with ModelSim*	**2:00 PM – 4:30 PM** **Session 6** 1. **Name of the Expert :** *Intel Technology India Private Limited* 2. **Designation** : *IP Engineer* 3. **Organization:***Intel Technology India Private Limited* 4. **Experience in Years:** *18* 5. **Topic to be taught:** *Working with Intel Quartus on SOC*	**2:00 PM – 4:30 PM** **Session 8** 1. **Name of the Expert :** *Padmanaban K* 2. **Designation** : *Software Enabling & Optimization Engineer* 3. **Organization:***Intel Technology India Private Limited* 4. **Experience in Years:** *18* 5. **Topic to be taught:** *Using Intel Tool for AI on FPGA*	**2:00 PM – 4:30 PM** **Session 9** 1. **Name of the Expert :** *Dr Nithish Kumarr.* 2. **Designation** Asso.Prof 3. **Organization:** VIT University,Vellore 4. **Experience in Year s**15 5. **Topic to be taught:** *Research Opportunities in FPGA Design*	**2:00 PM – 4:30 PM** **MCQ & Reflection Journal**
4:30 PM – 5:30 PM **Hands on training /Labs** 1. **Name of the Expert :** *Padmanaban K* *Dr Sanju*	**4:30 PM – 5:30 PM** **Hands on training /Labs** **Name of the Expert :** *Padmanaban K* *Dr Sanju*	**4:30 PM – 5:30 PM** **Hands on training /Labs** 1. **Name of the Expert :** *Dr Sanju*	**4:30 PM – 5:30 PM** **Hands on training /Labs** **Name of the Expert :** *Padmanaban K* *Dr Sanju*	**4:30 PM – 5:30 PM** **Hands on training /Labs** *Padmanaban K* *Dr Sanju*	**4:00 PM – 5:00 PM** **Valedictory Session**